CE transistor amplifier design

Below are two examples of transistor amplifier design operating in OE configuration.

The first task presents the design of a circuit whose task is to obtain a specified amplitude of undistorted sinusoidal voltage on a given value of the load resistance of the amplifier. In addition, the operating parameters of the circuit are determined and a method of limiting the operating bandwidth of the amplifier is given. Also analyzed is the change in the operating parameters of the circuit in the absence of the shunt capacitance of the emitter resistor (introduction of local feedback).

In task number 2, a transistor amplifier was designed to meet the following requirements: a specified voltage gain, noise characteristics (operating point selection) and a specified operating bandwidth of the system.

Task 1

Design a transistor amplifier operating in the OE configuration (Figure 1), whose minimum output voltage amplitude will be $U_{WYmin} = 1.5V$ for a circuit load resistance $R_L = 3k\Omega$. The lower frequency f_d should be 80Hz, and the upper frequency $f_g = 200kHz$. Determine the operating parameters and the upper limit frequency of the designed amplifier in the absence of capacitance C_3 in the circuit. In the circuit use transistor BC527 II with parameters: $U_{BE} = 0.65V$, $U_{Cesat} = 0.25V$, $\beta_0 = 200$, $c_{b'c} = 4.5pF$, $f_T = 150MHz$, $r_{bb'} = 0$. The resistance of the generator is equal to $R_g = 1k\Omega$. Normalize all determined values of resistance and capacitance to series E24.

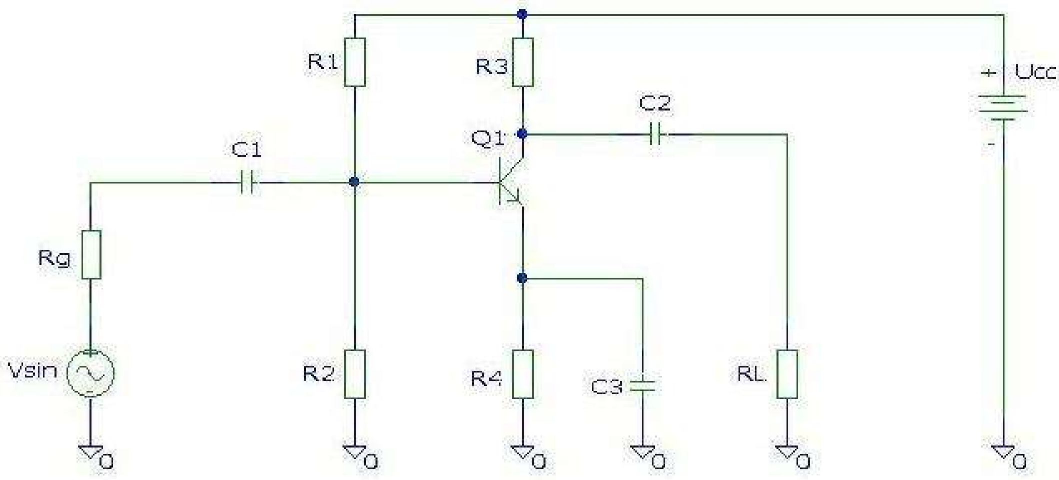

Fig. 1.1 Schematic of the designed transistor amplifier

Solution

In order to be able to obtain a certain value of undistorted voltage amplitude at the output of the amplifier, at a given value of load resistance, the operating point of the transistor (I_{CQ}, $U_{(CEQ)}$) must be selected accordingly. To determine the value of the collector current I_{CQ}, an alternating current analysis of the amplifier output will be helpful (Fig. 1.2).

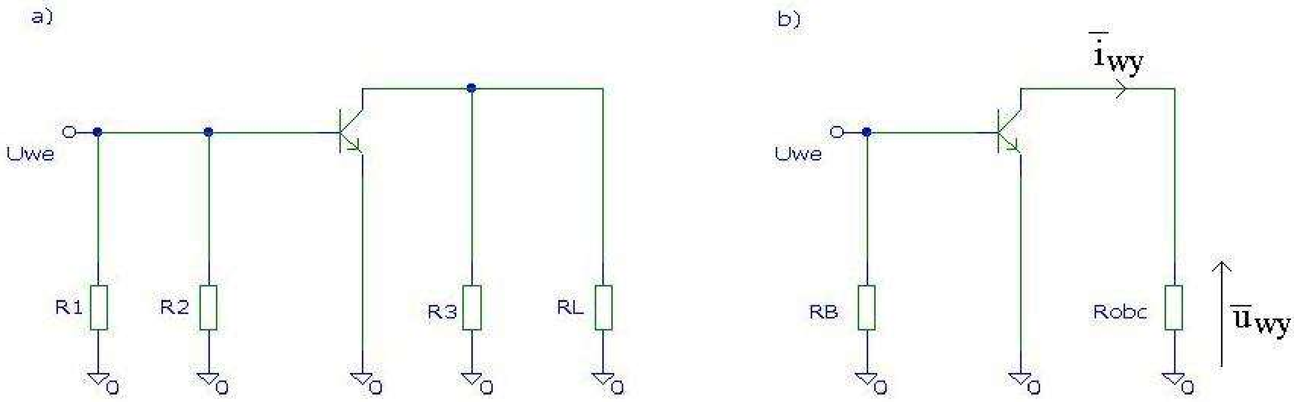

Figure 1.2: AC schematic of the amplifier: a) including all elements, b) simplified by including parallel connection of resistances

The resistances shown in Fig. 1.2b are given by the following relations:

$$R_B = R_1 \| R_2 \tag{1.1}$$

$$R_{obc} = R_3 \| R_L \ . \tag{1.2}$$

Analyzing the diagram in Fig. 1.2b, it can be written, using Ohm's law, that:

$$\bar{i}_{WY} = \frac{\bar{u}_{WY}}{R_{obc}} . \tag{1.3}$$

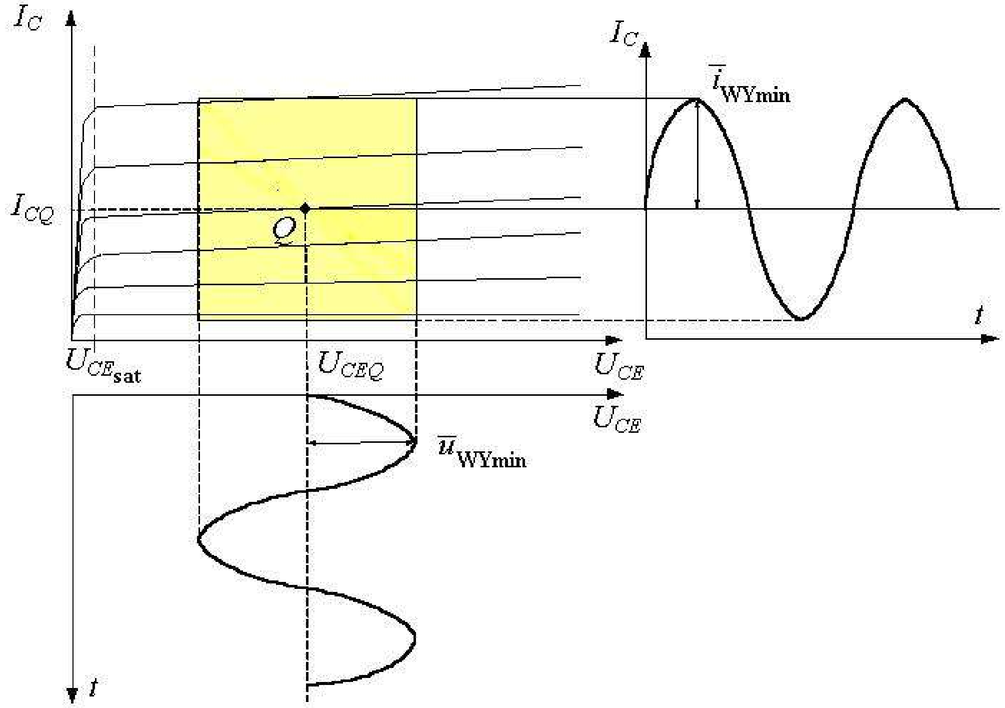

Figure 1.3: Output characteristics of the transistor with the operating point plotted and changes in voltage U_{CE} and current I_C

We also see from Fig. 1.3 that the maximum amplitude of the amplifier's output current i_{WY} is equal in value to that of the transistor at the operating point I_{CQ}. The currents i_{WY} and I_{CQ} have opposite returns. Using relation (1.3), we can determine the minimum value of the amplitude of the amplifier's output current and, consequently, the minimum value of the transistor's collector current at the operating point. Since we do not know the value of the load resistance R_{obc}, we must assume the value of the collector resistance R_3 before calculations. We assume the value of the resistance R_3 to be within single kilohms. For simplicity of calculation, $R_3 = R_L = 3k\Omega$ is assumed. Thus, using relation (1.2) $R_{obc} = 1.5k\Omega$ and the minimum value of the amplifier's output current amplitude is:

$$\bar{i}_{WY\min} = I_{CQ\min} = \frac{\bar{u}_{WY\min}}{R_{obc}} = \frac{1.5V}{1.5k\Omega} = 1mA \tag{1.4}$$

To meet the condition for the minimum amplitude of the undistorted output voltage of the amplifier with a certain margin, the value of the collector current of the transistor at the operating point $I_{CQ} = 1.5mA$ was assumed. The value of the collector-emitter voltage of the transistor at the operating point was determined using Fig. 1.3. To ensure that the transistor does not enter a saturated state for the specified minimum amplitude of the amplifier output voltage, the minimum value of the voltage U_{CEQ} must satisfy the relation:

$$U_{CEQ\,min} = U_{CEsat} + \bar{u}_{WY\,min} + \Delta U \tag{1.5}$$

where ΔU is a voltage reserve that takes into account changes in operating point caused by temperature changes. Usually it is assumed $\Delta U = (1 \div 2)V$. Assuming $\Delta U = 2V$ voltage U_{CEQmin} is:

$$U_{CEQ\,min} = U_{CEsat} + \bar{u}_{WY\,min} + \Delta U = 0.25V + 1.5V + 2V = 3.75V \tag{1.6}$$

Then, using the amplifier's DC schematic (Fig. 1.4), we determine the value of the amplifier supply voltage and the values of the other resistances in the circuit.

To ensure good temperature stability of the operating point, the voltage drop across the emitter resistor R_4 should be several times the base-emitter voltage of the transistor:

$$U_{R4} = (2 \div 4)U_{BEQ} \tag{1.7}$$

Using the above, we determine the value of the voltage U_{R3}:

$$U_{R4} = 3U_{BEQ} = 3 \cdot 0.65V = 1.95V \tag{1.8}$$

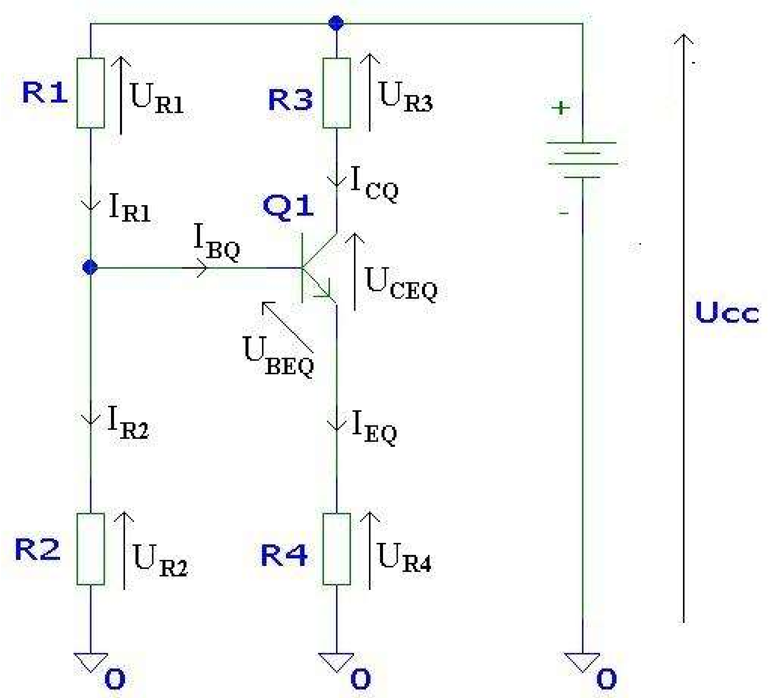

Figure 4: DC schematic of the amplifier

Then, the equation can be written:

$$U_{CC\,min} = U_{R3} + U_{CEQ\,min} + U_{R4} = I_{CQ}R_3 + U_{CEQ\,min} + U_{R4} = \\ = 1.5mA \cdot 3k\Omega + 3.75V + 1.95V = 10.2V \tag{1.9}$$

Normalizing the value of the supply voltage to standard values, $U_{CC} = 12V$ was assumed, which increased the collector-emitter voltage to $U_{CEQ} = 5.55V$.
Assuming that $I_{CQ} \cong I_{EQ}$, the value of the resistor R_4 can be determined:

$$R_4 = \frac{U_{R4}}{I_{CQ}} = \frac{1.95V}{1.5mA} = 1.3k\Omega \qquad (1.10)$$

We determine the value of the base current of the transistor I_{BQ} from the relation:

$$I_{BQ} = \frac{I_{CQ}}{\beta_0} = \frac{1.5mA}{200} = 7.5\mu A\,. \qquad (1.11)$$

To ensure good temperature stability of the operating point, it is assumed that the current division on the base divider is:

$$\frac{I_{R2}}{I_{BQ}} = (5 \div 20) \qquad (1.12)$$

Assuming that $I_{R2} = 10I_{BQ}$ we determine:

$$I_{R2} = 10 I_{BQ} = 75\mu A \qquad (1.13)$$

Using Kirchoff's 1st law, we can write that:

$$I_{R1} = I_{R2} + I_{BQ} = 11 I_{BQ} = 82.5\mu A \qquad (1.14)$$

Next, we determine the value of the resistor R_2:

$$R_2 = \frac{U_{R2}}{I_{R2}} = \frac{U_{BEQ} + U_{R4}}{I_{R2}} = \frac{2.6V}{75\mu A} = 34.666k\Omega \cong 36k\Omega \qquad (1.15)$$

We determine the resistor R_1 using the relationship:

$$R_1 = \frac{U_{R1}}{I_{R1}} = \frac{U_{CC} - U_{R2}}{I_{R1}} = \frac{U_{CC} - U_{BEQ} - U_{R4}}{I_{R1}} = \frac{9.4V}{82.5\mu A} = 113.939k\Omega \cong 110k\Omega \qquad (1.16)$$

Before determining the capacitance values of C_1, C_2 and C_3, the operating parameters of the amplifier must be determined.
Fig. 1.5 shows an alternating-current diagram of an amplifier with a transistor replaced by its π-hybrid model.

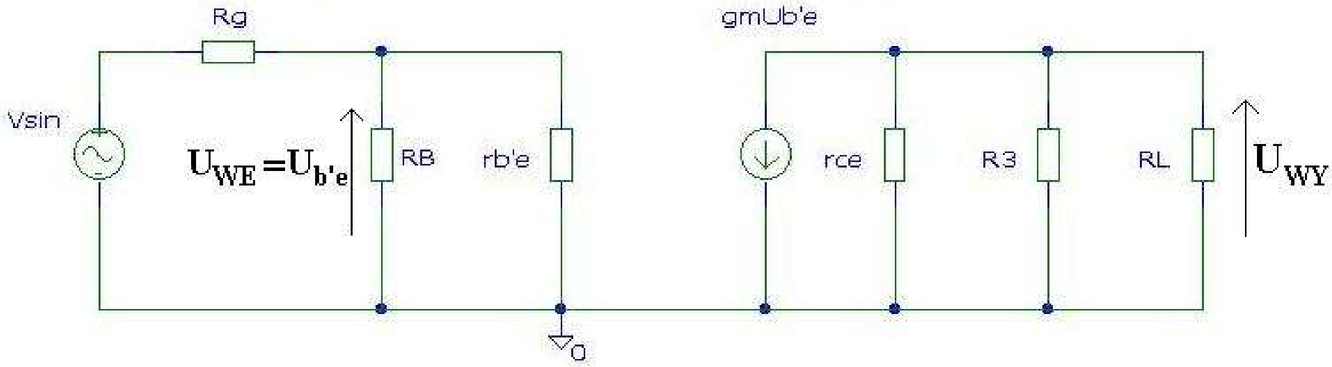

Figure 1.5: Variable-current diagram of the amplifier

If we have the exact catalog data of the transistor, then from the characteristics contained therein we can read the values of the individual elements of the transistor's π-hybrid model (in the Manual for the Laboratory Exercise these data are included in the accompanying table). When we have only the basic parameters, such as those given in the body of the task, the parameters of the π-hybrid model can be estimated using the knowledge of the working point of the transistor. Thus:

$$r_{b'e} = \frac{\beta_0 \varphi_T}{I_{CQ}} = \frac{200 \cdot 26.5mV}{1.5mA} = 3.53k\Omega \tag{1.17}$$

$$g_m = \frac{I_{CQ}}{\varphi_T} = \frac{1.5mA}{26.5mV} = 56.6mS \tag{1.18}$$

$$r_{ce} = \frac{U_Y}{I_{CQ}} = 66.6k\Omega \tag{1.19}$$

Where:

φ_T - is the thermal potential of the junction equal to 26.5mV at room temperature,

U_Y - this is Early's voltage equal to 100V for NPN transistors or 60V for PNP transistors.

The capacitance $c_{b'e}$, not marked in Figure 5, is determined by transforming the equation:

$$f_T = \frac{g_m}{2\pi(c_{b'e} + c_{b'c})} \tag{1.20}$$

And so, based on the catalog data of transistor BC527 II given in the body of the task:

$$c_{b'e} = \frac{g_m}{2\pi f_T} - c_{b'c} = \frac{56.6mS}{2 \cdot \pi \cdot 150MHz} - 4.5pF = 55.5pF \tag{1.21}$$

We determine the voltage gain of the system using the relationship:

$$k_U = -g_m \left(R_{obc} \| r_{ce}\right) = -56.6mS \cdot 1.46k\Omega = -83\left[\frac{V}{V}\right] \tag{1.22}$$

The input resistance of the amplifier is given by the relation:

$$r_{WE} = R_B \| r_{b'e} = 3.123k\Omega \tag{1.23}$$

The output resistance of the circuit is equal to:

$$r_{WY} = R_3 \| r_{ce} = 2.87k\Omega \tag{1.24}$$

The generator voltage utilization factor is:

$$\gamma_U = \frac{r_{WE}}{R_g + r_{WE}} = \frac{3.123k\Omega}{1k\Omega + 3.123k\Omega} = 0.757 \tag{1.25}$$

The effective voltage gain of the system is given by the relation:

$$k_{USK} = \gamma_U k_U = -62.87\left[\frac{V}{V}\right] \tag{1.26}$$

We will determine the upper limit frequency of the amplifier using the circuit's alternating-current schematic, with the transistor replaced by its full π-hybrid model (taking into account capacitances $c_{b'e}$ and $c_{b'c}$, with $r_{bb'} = 0$). This schematic is shown in Figure 1.6.

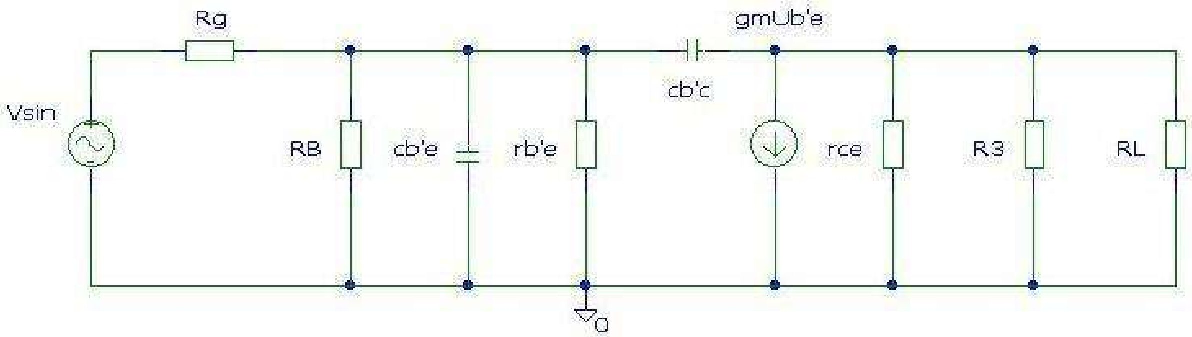

Figure 1.6: Schematic of amplifier with transistor replaced by full model of π-hybrids

Using Miller's voltage theorem, we transform the system to the form shown in Fig. 1.7.

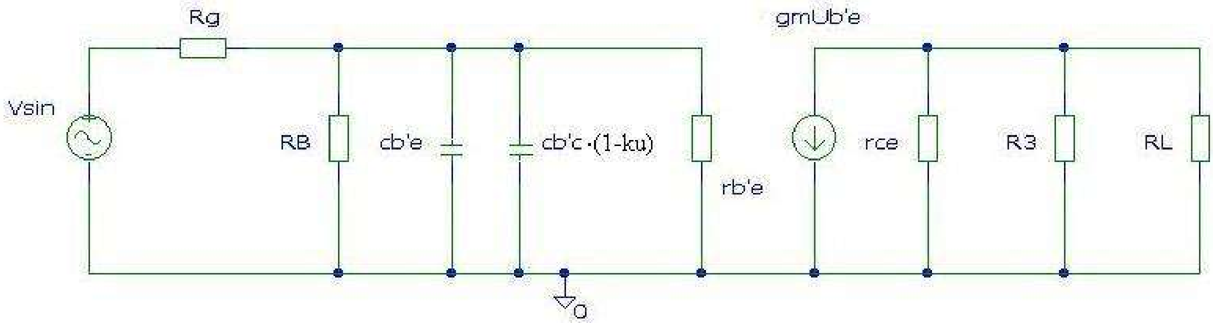

Figure 1.7: Variable-signal diagram of the amplifier after applying Miller's theorem

Determining the top frequency of the amplifier boils down to determining the limiting frequency of the circuit shown in Fig. 1.8:

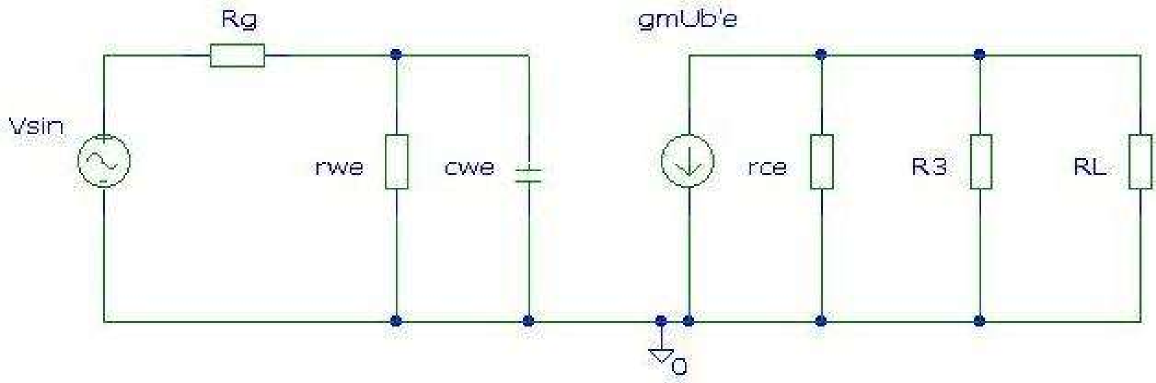

Figure 1.8: Amplifier schematic to help determine the upper frequency of the system

The input capacitance of the system is given by the relation:

$$c_{WE} = c_{b'e} + (1 - k_U)c_{b'c} = 55.5pF + 378pF = 433.5pF \tag{1.27}$$

The voltage transmittance of the amplifier in Fig. 1.8 is given by the relation:

$$k_{USK}(s) = -g_m(R_{obc} \| r_{ce}) \left(\frac{r_{WE} \left\| \frac{1}{sc_{WE}} \right.}{R_g + r_{WE} \left\| \frac{1}{sc_{WE}} \right.} \right) = k_U \left(\frac{r_{WE} \left\| \frac{1}{sc_{WE}} \right.}{R_g + r_{WE} \left\| \frac{1}{sc_{WE}} \right.} \right) \tag{1.28}$$

Where . $s = j\omega = j2\pi f$

After transformations, the relation (1.28) takes the form:

$$k_{USK}(s) = \frac{k_U}{sR_g c_{WE} + \frac{R_g}{r_{WE}} + 1} \tag{1.29}$$

Finding the upper limit frequency of the system involves solving the equation:

$$sR_g c_{WE} + \frac{R_g}{r_{WE}} + 1 = 0 \tag{1.30}$$

Finally, the limiting frequency of the amplifier is:

$$f_g = \frac{\frac{R_g}{r_{WE}} + 1}{2\pi R_g c_{WE}} = \frac{\frac{1k\Omega}{3.123k\Omega} + 1}{2 \cdot \pi \cdot 1k\Omega \cdot 433.5pF} = 484.624kHz \tag{1.31}$$

To limit the upper frequency of the amplifier to 200kHz, an additional capacitance C_d must be connected between the base and collector of the transistor. In the amplifier model shown in Fig. 1.6, this capacitance is added to the capacitance $c_{(b'c)}$ of the transistor, so that the final formula for the input capacitance of the circuit c_{WE} (Fig. 1.8) will be:

$$c_{WE} = c_{b'e} + (1 - k_U)(c_{b'c} + C_d) \tag{1.32}$$

To determine the value of capacitance C_d, for which the upper frequency of the amplifier will be equal to 200 kHz, it is necessary, taking into account equation (1.32), to transform the relation (1.31). Thus, the capacitance C_d will be given by the relation:

$$C_d = \frac{\frac{R_g}{r_{WE}} + 1}{2\pi f_g R_g (1 - k_U)} - \frac{c_{b'e}}{1 - k_U} - c_{b'c} = \frac{\frac{1k\Omega}{3.123k\Omega} + 1}{2 \cdot \pi \cdot 200kHz \cdot 1k\Omega \cdot 84} - \frac{55.5pF}{84} - 4.5pF = 7.34pF \cong 7.5pF$$

Capacitances C_1, C_2 and C_3 can be determined by knowing the value of the lower frequency f_d of the amplifier. The voltage transmittance of an amplifier in the low frequency range has three poles s_1, s_2 and s_3. Assuming that these poles are independent of each other, the lower frequency of the amplifier can be determined from the relation:

$$f_d = \sqrt{f_1^2 + f_2^2 + f_3^2} \tag{1.33}$$

where the frequencies f_1, f_2 and f_3 are related to the mentioned poles by the relation $f_n = \left|\frac{s_n}{2\pi}\right|, n = 1,2,3$. The values of each frequency are functions of the capacitances C_1, C_2 and C_3.

$$f_1 = \frac{1}{2\pi C_1 (r_{WE} + R_g)} \tag{1.34}$$

$$f_2 = \frac{1}{2\pi C_2 (r_{WY} + R_L)} \tag{1.35}$$

$$f_3 = \frac{1 + \frac{(\beta_0 + 1)R_4}{R_g \| R_B + r_{b'e}}}{2\pi R_4 C_3} \tag{1.36}$$

In order to achieve good stability of the amplifier in the lower frequencies, the poles must be properly arranged on the frequency axis (separated). It is usually assumed that the pole caused by the emitter capacitance C_3 is the dominant pole (having the greatest influence on the value of the cutoff frequency), while the other poles are much smaller than it:

$$f_3 >> f_1 > f_2 \tag{1.37}$$

And so, for example, you can assume the following relationships between the different frequencies: $f_1 = \frac{f_3}{10}$, $f_2 = \frac{f}{15}$. Then the relation (1.33) will take the form:

$$f_d = \sqrt{\left(\frac{f_3}{10}\right)^2 + f_3^2 + \left(\frac{f_3}{15}\right)^2} = 1.08 f_3 .$$

After the transformation, we get:

$$f_3 = \frac{f_d}{1.007} = 79.44Hz \tag{1.38}$$

The other frequencies take values: $f_1 = 7.944Hz, f_2 = 5.29Hz$ .After transforming the relationship (1.34) - (1.36), we can determine the values of capacitances C_1 - C_3:

$$C_1 = \frac{1}{2\pi f_1 \left(r_{WE} + R_g\right)} = 4.85\mu F \cong 4.7\mu F \tag{1.39}$$

$$C_2 = \frac{1}{2\pi f_2 \left(r_{WY} + R_L\right)} = 5.11\mu F \cong 5.6\mu F \tag{1.40}$$

$$C_3 = \frac{1 + \dfrac{(\beta_0 + 1)R_4}{R_g \| R_B + r_{b'e}}}{2\pi f_3 R_4} = 91\mu F \cong 100\mu F \tag{1.41}$$

When there is no capacitance C_3 in the designed amplifier, the amplifier is covered by a current-array feedback loop realized with an emitter resistor R_4. Then the operating parameters of the circuit are given by the relations:

$$k_{Uf} \cong -\frac{r_{ce} \| R_{obc}}{R_4} = -1.12\left[\frac{V}{V}\right] \tag{1.42}$$

$$r_{WEf} = R_B \| \left[r_{b'e}\left(1 + g_m R_4\right)\right] = 24.58k\Omega \tag{1.43}$$

$$r_{WYf} \cong R_3 = 3k\Omega \tag{1.44}$$

$$\gamma_{Uf} = \frac{r_{WEf}}{R_g + r_{WEf}} = 0.96 \tag{1.45}$$

$$k_{USKf} = \gamma_{Uf} k_{Uf} = -1.07\left[\frac{V}{V}\right] \tag{1.46}$$

The upper limit frequency of a feedback amplifier can be calculated using the relationship:

$$f_{gf} = \frac{\dfrac{R_g}{\left(r_{b'e} + \beta_0 R_4\right) \| R_B} + 1}{2\pi R_g \left[c_{b'e} \dfrac{r_{b'e}}{r_{b'e} + \beta_0 R_4} + \left(1 + \dfrac{r_{b'e}}{r_{b'e} + \beta_0 R_4} g_m \left(r_{ce} \| R_{obc}\right)\right) c_{b'c}\right]} = 6.343MHz \tag{1.47}$$

We will determine the lower limiting frequency from the relationship:

$$f_{df} = \sqrt{f_{1f}^2 + f_{2f}^2} = 36.33Hz \tag{1.48}$$

Where:

$$f_{1f} = \frac{1}{2\pi C_1 \left(R_g + r_{WEf}\right)} = 36.05Hz \tag{1.49}$$

$$f_{2f} = \frac{1}{2\pi C_2 \left(r_{WYf} + R_L\right)} = 4.73Hz \tag{1.50}$$

Task 2

Design a low-noise, acoustic (20Hz - 20kHz bandwidth) transistor amplifier with a voltage gain of -10V/V, operating in an OE configuration, on a BC527 II transistor with parameters: U_{BE} = 0.65V, U_{Cesat} = 0.25V, β_0 = 200, $c_{b'c}$ = 4.5pF, f_T = 150MHz, $r_{bb'}$ = 0. The circuit diagram is shown in Figure 1. The amplifier will operate with a load resistance equal to 5.1 kΩ. The resistance of the generator is equal to 600Ω. Give the maximum value of the undistorted amplitude of the output voltage of the circuit.

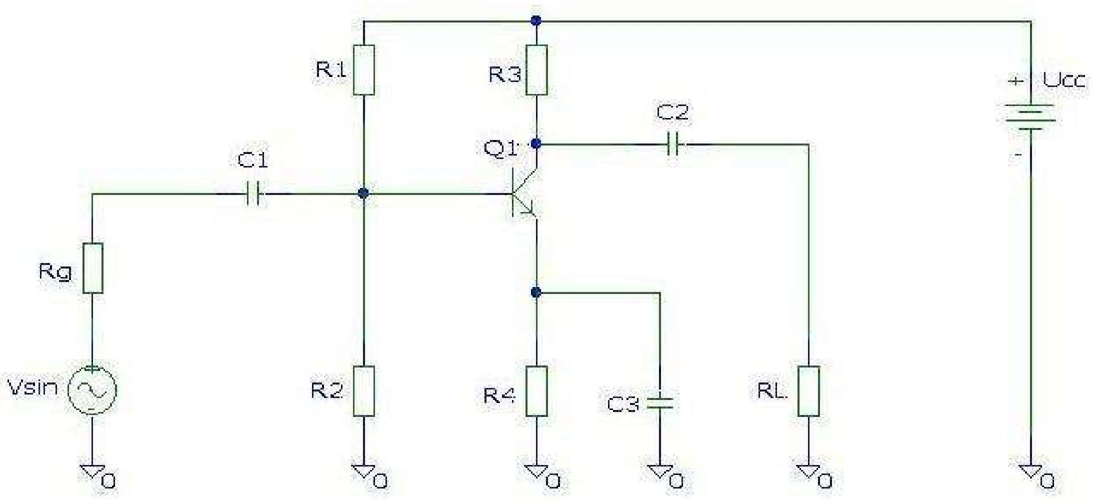

Figure 2.1: Schematic of a transistor amplifier

Solution

If the amplifier is to be characterized by low noise, the operating point of the transistor should be selected accordingly (see Table Lecture No. 4 UE1). The collector current of the transistor at the operating point should be in the range I_{CQ} = (20 - 200)μA (when there is no requirement for circuit noise parameters, the collector current is selected from the range $I_{(CQ)}$ = (1 - 5)mA)). Meanwhile, the collector-emitter voltage U_{CEQ} should take values in the range of (1 - 5)V. We tentatively assume I_{CQ} = 100μA, U_{CEQ} = 5V. We will carry out further calculations using the alternating-current schematic of the amplifier in which the transistor is replaced by its small-signal model of π-hybrids (Fig. 2.2).

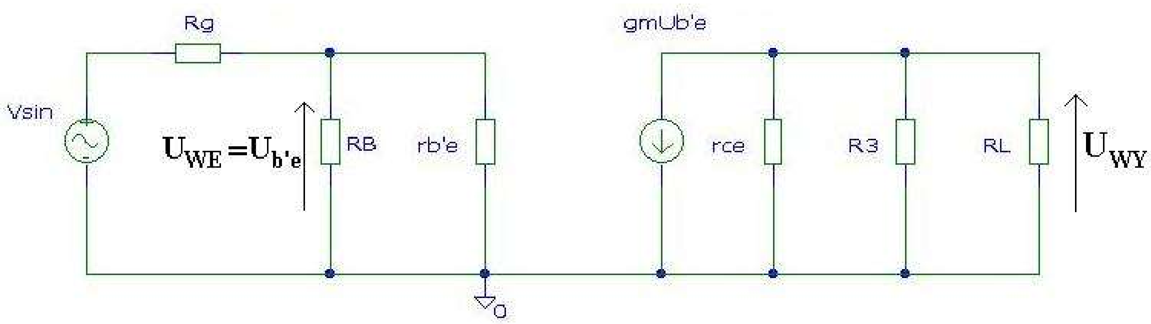

Figure 2.2: Variable-current diagram of the amplifier

The voltage gain of the OE system is expressed by the relation:

$$k_U = -g_m\left(r_{ce}\|R_3\|R_L\right) \tag{2.1}$$

If we have the exact catalog data of the transistor used in the amplifier, then for a given collector current at the operating point, we find the parameters of the π-hybrid model (in the Laboratory Exercise Manual, these data are included in the accompanying table). However, if we only know the basic parameters of the transistor, as in the task being solved, we can use simplified relationships and determine the approximate values of the elements of the small-signal model of the transistor:

$$r_{b'e} = \frac{\beta_0 \varphi_T}{I_{CQ}} = \frac{200 \cdot 26.5mV}{0.1mA} = 53k\Omega \tag{2.2}$$

$$g_m = \frac{I_{CQ}}{\varphi_T} = \frac{0.1mA}{26.5mV} = 3.77mS \tag{2.3}$$

$$r_{ce} = \frac{U_Y}{I_{CQ}} = \frac{100V}{0.1mA} = 1M\Omega \tag{2.4}$$

Where:
φ_T - is the thermal potential of the junction equal to 26.5mV at room temperature,
U_Y - this is Early's voltage equal to 100V for NPN transistors or 60V for PNP transistors.
The capacity $c_{b'e}$, not marked in Fig. 2.2, is determined by transforming the equation:

$$f_T = \frac{g_m}{2\pi\left(c_{b'e} + c_{b'c}\right)} \tag{2.5}$$

And so, based on the catalog data of transistor BC527 II given in the body of the task:

$$c_{b'e} = \frac{g_m}{2\pi f_T} - c_{b'c} = \frac{56.6mS}{2 \cdot \pi \cdot 150MHz} - 4.5pF = -0.5pF$$

The determined value is, of course, unrealistic (capacitance cannot take negative values). The negative value of the capacitance indicates that the capacitance $c_{b'e}$ can be ignored in further calculations.

Having calculated small-signal parameters of the transistor, we can determine, by transforming relation (1), the value of collector resistance R_3:

$$R_3 = \left(\frac{g_m}{k_U} - r_{ce}^{-1} - R_L^{-1}\right)^{-1} = \left(\frac{3.77mS}{10\left[\frac{V}{V}\right]} - (1M\Omega)^{-1} - (5.1k\Omega)^{-1}\right)^{-1} = 5.55k\Omega \cong 5.6k\Omega \tag{2.5}$$

We will determine the remaining resistors based on the DC scheme shown in Figure 2.3.
To ensure good temperature stability of the operating point, the voltage drop across the emitter resistor R_4 should be several times the base-emitter voltage of the transistor:

$$U_{R4} = (2 \div 4)U_{BEQ} \tag{2.6}$$

Using the above, we determine the value of the voltage U_{R4}:

$$U_{R4} = 2U_{BEQ} = 2 \cdot 0.65V = 1.3V \tag{2.7}$$

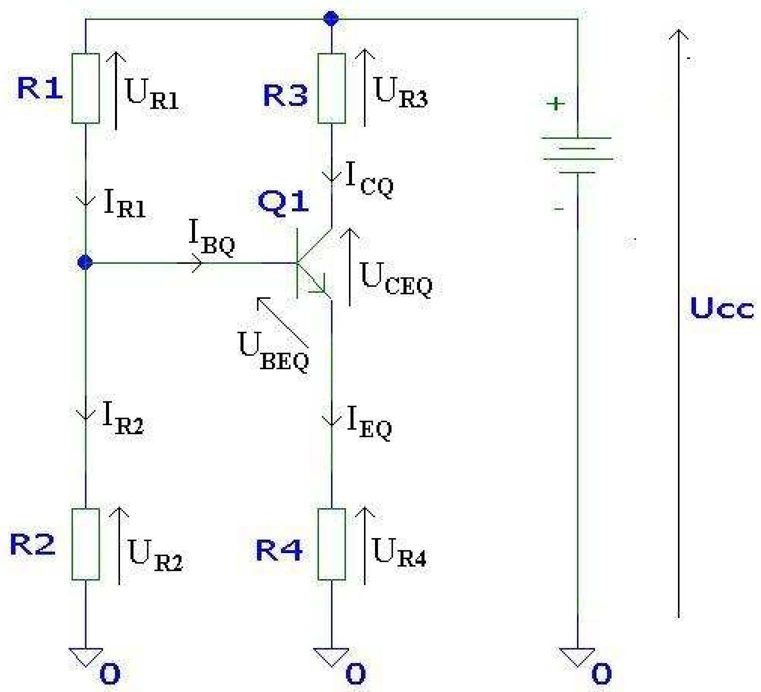

Figure 2.3: DC schematic of the amplifier

Then, the equation can be written:

$$U_{CC} = U_{R3} + U_{CEQ} + U_{R4} = I_{CQ}R_3 + U_{CEQ} + U_{R4} = \\ = 0.1mA \cdot 5.6k\Omega + 5V + 1.3V = 6.86V \tag{2.8}$$

Normalizing the supply voltage to standard values, $U_{CC} = 5V$ was assumed, which will cause the collector-emitter voltage to drop to $U_{CEQ} = 3.14V$. This value is still within the range of collector-emitter voltages for low-noise amplifiers.

Assuming that $I_{CQ} \cong I_{EQ}$, the value of the resistor R_4 can be determined:

$$R_4 = \frac{U_{R4}}{I_{CQ}} = \frac{1.3V}{0.1mA} = 13k\Omega \tag{2.9}$$

We determine the value of the base current of the transistor I_{BQ} from the relation:

$$I_{BQ} = \frac{I_{CQ}}{\beta_0} = \frac{0.1mA}{200} = 0.5\mu A\,. \tag{2.10}$$

To ensure good temperature stability of the operating point, it is assumed that the current division on the base divider is:

$$\frac{I_{R2}}{I_{BQ}} = (5 \div 20) \tag{2.11}$$

Assuming that $I_{R2} = 10I_{BQ}$ we determine:

$$I_{R2} = 10 I_{BQ} = 5\mu A \qquad (2.12)$$

Using Kirchoff's 1st law, we can write that:

$$I_{R1} = I_{R2} + I_{BQ} = 11 I_{BQ} = 5.5\mu A \qquad (2.13)$$

Then we determine the value of the resistor R_2:

$$R_2 = \frac{U_{R2}}{I_{R2}} = \frac{U_{BEQ} + U_{R4}}{I_{R2}} = \frac{1.95V}{5\mu A} = 390k\Omega \qquad (2.14)$$

We determine the resistor R_1 using the relationship:

$$R_1 = \frac{U_{R1}}{I_{R1}} = \frac{U_{CC} - U_{R2}}{I_{R1}} = \frac{U_{CC} - U_{BEQ} - U_{R4}}{I_{R1}} = \frac{3.05V}{5.5\mu A} = 554.545k\Omega \cong 560k\Omega \qquad (2.15)$$

Now the remaining operating parameters of the system can be determined, again using Fig. 2.2.
The input resistance of the amplifier is given by the relation:

$$r_{WE} = R_B \| r_{b'e} = 43k\Omega \qquad (2.16)$$

The output resistance of the circuit is equal to:

$$r_{WY} = R_3 \| r_{ce} = 5.57k\Omega \qquad (2.17)$$

The generator voltage utilization factor is:

$$\gamma_U = \frac{r_{WE}}{R_g + r_{WE}} = \frac{43k\Omega}{0.6k\Omega + 43k\Omega} = 0.986 \qquad (2.18)$$

The effective voltage gain of the system is given by the relation:

$$k_{USK} = \gamma_U k_U = -9.86 \left[\frac{V}{V}\right] \qquad (2.19)$$

We will determine the upper limit frequency of the amplifier using the circuit's alternating-current schematic, with the transistor replaced by its full π-hybrid model (taking into account capacitances $c_{b'e} = 0$ and $c_{b'c}$, with $r_{bb'} = 0$). This schematic is shown in Figure 2.4.

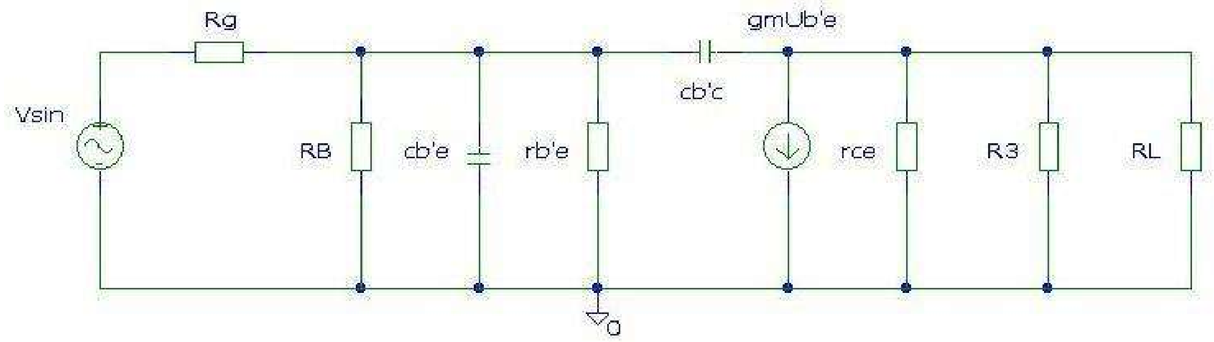

Figure 2.4: Schematic of amplifier with transistor replaced by full model of π-hybrids

Using Miller's voltage theorem, we transform the system to the form shown in Fig. 2.5.

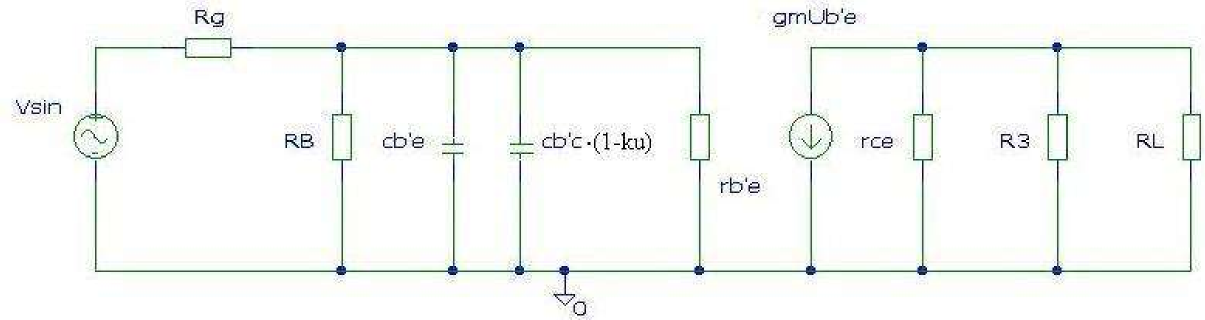

Figure 2.5: Variable-signal diagram of the amplifier after applying Miller's theorem

Determining the top frequency of the amplifier boils down to determining the limiting frequency of the circuit shown in Fig. 2.6:

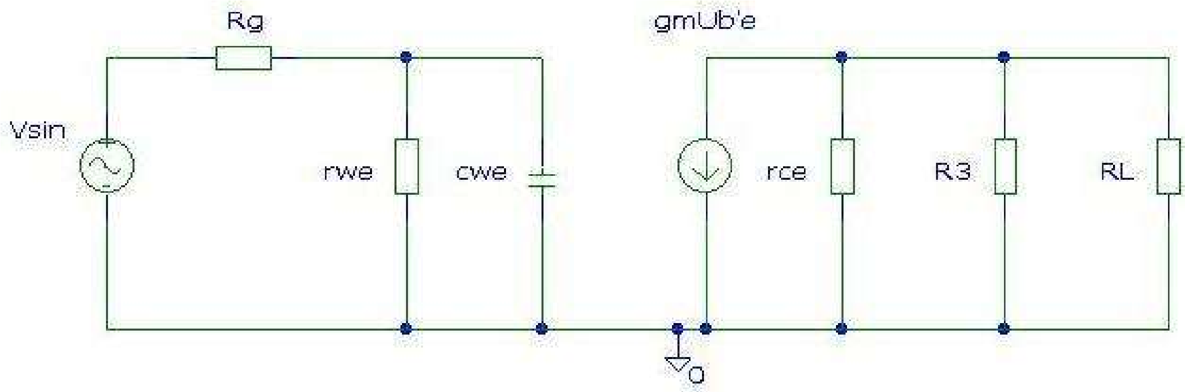

Figure 2.6: Amplifier schematic to help determine the upper frequency of the system

The input capacitance of the system is given by the relation (with $c_{b'e}$ negligibly small):

$$c_{WE} = c_{b'e} + (1 - k_U)c_{b'c} = 0\,pF + 49.5\,pF = 49.5\,pF \tag{2.20}$$

The voltage transmittance of the amplifier in Fig. 2.6 is given by the relation:

$$k_{USK}(s) = -g_m\left(R_{obc} \| r_{ce}\right)\left(\frac{r_{WE} \left\| \frac{1}{sc_{WE}}\right.}{R_g + r_{WE} \left\| \frac{1}{sc_{WE}}\right.}\right) = k_U\left(\frac{r_{WE} \left\| \frac{1}{sc_{WE}}\right.}{R_g + r_{WE} \left\| \frac{1}{sc_{WE}}\right.}\right) \tag{2.21}$$

Where . $s = j\omega = j2\pi f$

After transformations, the relation (2.21) takes the form:

$$k_{USK}(s) = \frac{k_U}{sR_g c_{WE} + \frac{R_g}{r_{WE}} + 1} \tag{2.22}$$

Finding the upper limit frequency of the system involves solving the equation:

$$sR_g c_{WE} + \frac{R_g}{r_{WE}} + 1 = 0 \tag{2.23}$$

Finally, the limiting frequency of the amplifier is:

$$f_g = \frac{\frac{R_g}{r_{WE}} + 1}{2\pi R_g c_{WE}} = \frac{\frac{0.6k\Omega}{43k\Omega} + 1}{2 \cdot \pi \cdot 0.6k\Omega \cdot 49.5pF} = 5.432MHz \tag{2.24}$$

To limit the upper frequency of the amplifier to 20kHz, an additional capacitance C_d must be connected between the base and collector of the transistor. In the amplifier model shown in Fig. 2.4, this capacitance is added to the capacitance $c_{(b'c)}$ of the transistor, so that the final formula for the input capacitance of the circuit c_{WE} (Fig. 2.6) will be:

$$c_{WE} = c_{b'e} + (1 - k_U)(c_{b'c} + C_d) \tag{2.25}$$

To determine the value of capacitance C_d, for which the upper frequency of the amplifier will be equal to 20 kHz, it is necessary, taking into account equation (2.25), to transform the relation (2.24). Thus, the capacitance C_d will be given by the relation:

$$C_d = \frac{\frac{R_g}{r_{WE}} + 1}{2\pi f_g R_g (1 - k_U)} - \frac{c_{b'e}}{1 - k_U} - c_{b'c} = \frac{\frac{0.6k\Omega}{43k\Omega} + 1}{2 \cdot \pi \cdot 20kHz \cdot 0.6k\Omega \cdot 11} - \frac{0pF}{11} - 4.5pF = 1.22F \cong 1.2nF$$

Capacitances C_1, C_2 and C_3 can be determined by knowing the value of the lower frequency f_d of the amplifier. The voltage transmittance of an amplifier in the low frequency range has three poles s_1, s_2 and s_3. Assuming that these poles are independent of each other, the lower frequency of the amplifier can be determined from the relation:

$$f_d = \sqrt{f_1^2 + f_2^2 + f_3^2} \tag{2.26}$$

where the frequencies f_1, f_2 and f_3 are related to the mentioned poles by the relation $f_n = \left|\frac{s_n}{2\pi}\right|, n = 1,2,3$. The values of each frequency are functions of the capacitances C_1, C_2 and C_3.

$$f_1 = \frac{1}{2\pi C_1 \left(r_{WE} + R_g\right)} \tag{2.27}$$

$$f_2 = \frac{1}{2\pi C_2 \left(r_{WY} + R_L\right)} \tag{2.28}$$

$$f_3 = \frac{1 + \frac{(\beta_0 + 1)R_4}{R_g \| R_B + r_{b'e}}}{2\pi R_4 C_3} \tag{2.29}$$

In order to achieve good stability of the amplifier in the lower frequencies, the poles must be properly arranged on the frequency axis (separated). It is usually assumed that the pole caused by the emitter capacitance C_3 is the dominant pole (having the greatest influence on the value of the cutoff frequency), while the other poles are much smaller than it:

$$f_3 >> f_1 > f_2 \tag{2.30}$$

And so, for example, you can assume the following relationships between the different frequencies: $f_1 = \frac{f_3}{10}$, $f_2 = \frac{f}{15}$. Then the relation (12.26) will take the form:

$$f_d = \sqrt{\left(\frac{f_3}{10}\right)^2 + f_3^2 + \left(\frac{f_3}{15}\right)^2} = 1.007 f_3 .$$

After the transformation, we get:

$$f_3 = \frac{f_d}{1.007} = 19.86 Hz \tag{2.31}$$

The other frequencies take the values: $f_1 = 1.986 Hz, f_2 = 1.324 Hz$. After transforming the relationship (2.27) - (2.29), we can determine the values of capacitances C_1 - C_3:

$$C_1 = \frac{1}{2\pi f_1 \left(r_{WE} + R_g\right)} = 1.83 \mu F \cong 2.2 \mu F \tag{2.32}$$

$$C_2 = \frac{1}{2\pi f_2 \left(r_{WY} + R_L\right)} = 11.2 \mu F \cong 15 \mu F \tag{2.33}$$

$$C_3 = \frac{1 + \frac{(\beta_0 + 1)R_4}{R_g \| R_B + r_{b'e}}}{2\pi f_3 R_4} = 30.6\mu F \cong 33\mu F \tag{2.34}$$

The last thing to determine is to determine the maximum undistorted amplitude of the output voltage of the amplifier. Figure 2.7 will be helpful for the calculation. The maximum amplitude of the output voltage is limited by two phenomena: saturation and cutoff of the transistor. Saturation of the transistor occurs when the voltage $U_{CE} \leq U_{Cesat}$. This results in the condition for the maximum amplitude of the output voltage:

$$\bar{u}_{WY\max} = U_{CEQ} - U_{CEsat} = 3.14V - 0.25V = 2.89V \tag{2.35}$$

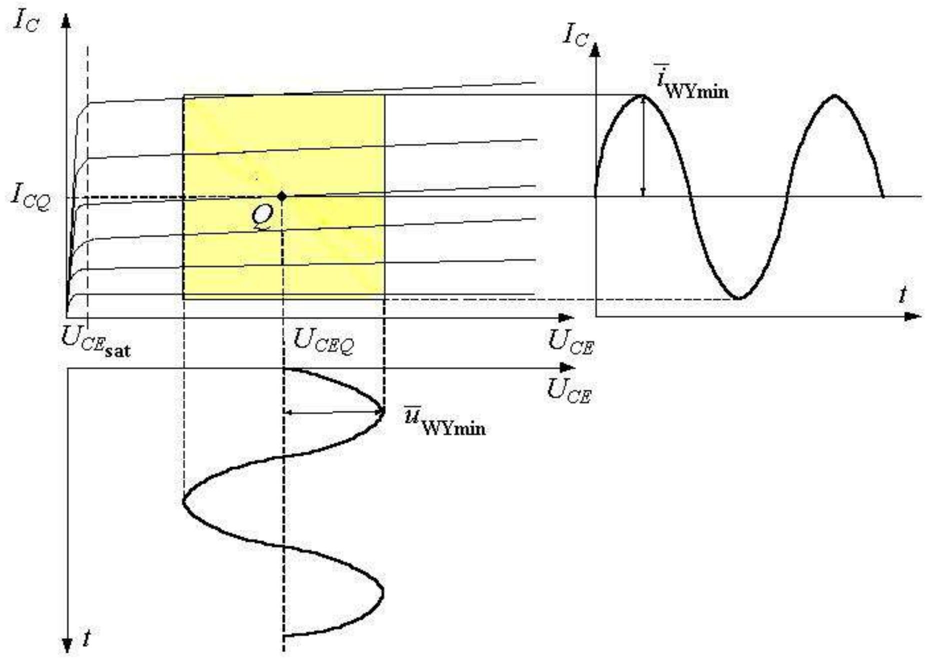

Figure 2.7: Output characteristics of the transistor with the operating point plotted and changes in voltage U_{CE} and current $I_{(C}$

On the other hand, the transistor is cut off when $I_C \leq 0$. This happens when the amplitude of the output current i_{WY} is greater than the value of the collector current of the transistor at the operating point I_{CQ}. That is, the maximum undistorted amplitude of the amplifier's output current is given by the expression . $\bar{i}_{WY\max} = I_{CQ}$

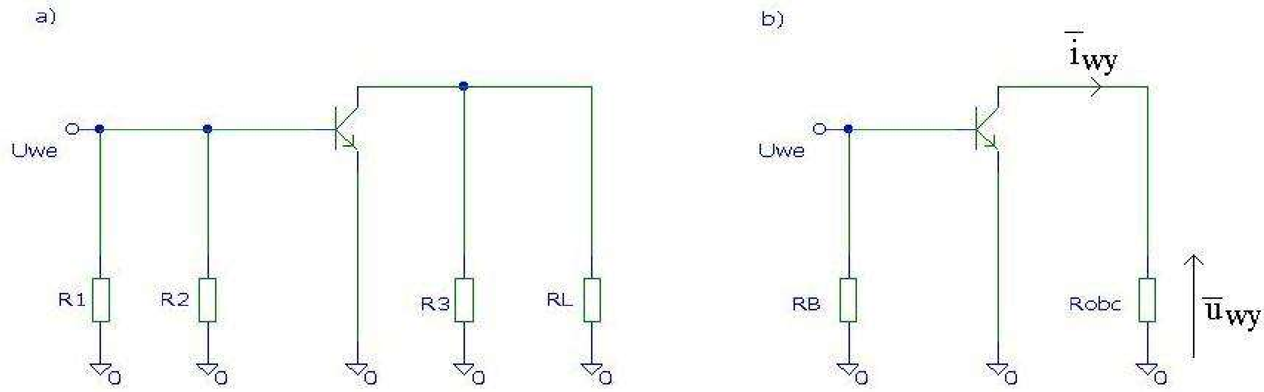

Figure 2.8: AC schematic of the amplifier: a) including all elements, b) simplified by including parallel connection of resistances

Using Ohm's law, it can be written that (Fig.2.8):

$$\bar{u}_{WY} = \bar{i}_{WY} R_{obc} \tag{2.36}$$

Then:

$$\bar{u}_{Wy\max} = \bar{i}_{WY\max} R_{obc} = I_{CQ} R_{obc} = I_{CQ}\left(R_3 \| R_L\right) = 0.1mA \cdot 2.669k\Omega = 0.266V \tag{2.37}$$

We obtained two values determining the maximum amplitude of the amplifier's output voltage:

- exceeding which causes saturation of the transistor - 2.89V
- exceeding which causes the transistor to cut off - 0.266V.

The value sought is, of course, the smaller of the amplitudes, i.e., ultimately we can write that:

$$\bar{u}_{WY\max} = 0.266V$$