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EMC basic aspects 3

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References

1. Williams T., *EMC for Product Designers*, Elsevier-Newnes, 5th ed., Oxford, 2015
2. Ott H. W., *Electromagnetic Compatibility Engineering*, Wiley, Hoboken, NJ, 2009

Illustrations in this presentation are taken mostly from above

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e) • use properly designed looms, ribbon or flexi for internal wiring – avoid loose wires or bundles
f) • run cables away from apertures in the shielding, tied close to conductive grounded structures
g) • apply ferrite suppressors to damp resonances and control common mode currents
h) • ensure that cable screens are properly terminated to the connector backshell; avoid pigtails
i) • terminate lines carrying high frequency signals with the correct transmission line impedance

6. • Grounding:
   a) • design and enforce the ground system at the product definition stage
   b) • consider the ground system as a return current path, not just as 0V reference
   c) • provide for parallel earth conductors at the system level
   d) • ensure metal-to-metal bonding of screens, connectors, filters, and enclosure panels • ensure that bonding methods will not deteriorate in adverse environments
   e) • mask paint from, and apply a conductive finish to, any intended contact surfaces • keep earth straps short and define their geometry
   f) • avoid common ground impedances for different circuits • provide an interface ground area for decoupling and filtering
7. • Filters:
   a) • assume that a supply filter is needed: design the filter for the application
   b) • filter all I/O lines, using either or both of three-terminal capacitors to interface ground, and common mode chokes
   c) • apply π filters at the DC power input to each board, in multi-board designs
   d) • ensure a defined ground return for each filter
   e) • apply filtering to interference sources, such as switches or motors, directly at their terminals
   f) • locate all filter components and associated wiring or tracks adjacent to the interface being filtered
8. • Shielding:
   a) • design all metallic structures as if they were electrical components: account for their stray capacitance and inductance
   b) • consider segregated enclosures: enclose particularly sensitive or noisy areas with extra internal shielding
   c) • avoid large or resonant apertures in a shield, or take measures to mitigate them
   d) • avoid dipole-like structures in a metallic enclosure
   e) • ensure that separate panels are well bonded along their seams using conductive gaskets: apply good bonding practice as in "grounding" above

Design checklist to assess your design against EMC.
TIP 6:

6.• Grounding:

a)• design and enforce the ground system at the product definition stage

b)• consider the ground system as a return current path, not just as 0V reference

c)• provide for parallel earth conductors at the system level

d)• ensure metal-to-metal bonding of screens, connectors, filters, and enclosure panels; ensure that bonding methods will not deteriorate in adverse environments

e)• mask paint from, and apply a conductive finish to, any intended contact surfaces; keep earth straps short and define their geometry

f)• avoid common ground impedances for different circuits; provide an interface ground area for decoupling and filtering

4

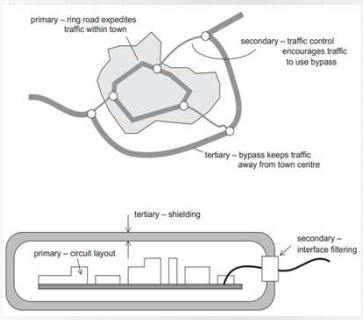
GROUNDING vs. EARTHING

grounding (USA)

give a reference potential (0V) for external connections to the system
a low impedance path by which current can return to its source

connection to the earth for safety purposes
Yelow-green cabel

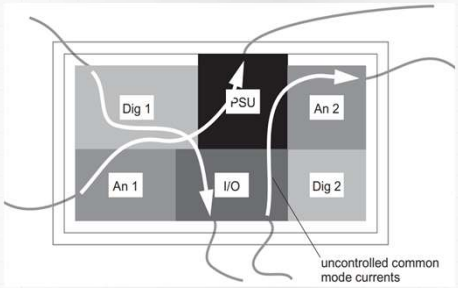
5

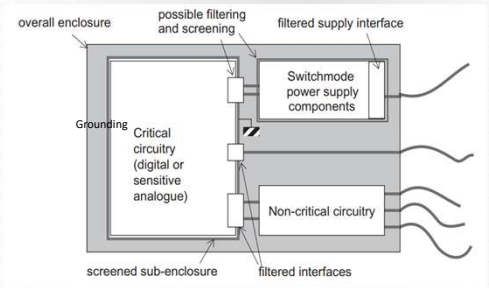


Not only the 0V reference, but also the return current

6

System partitioning

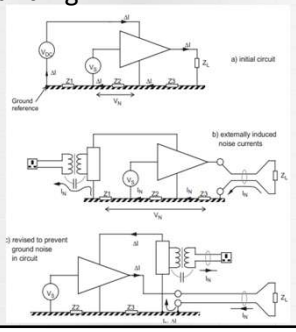




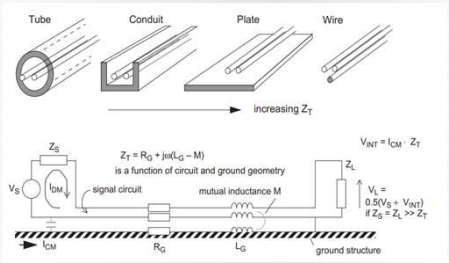
Grounding

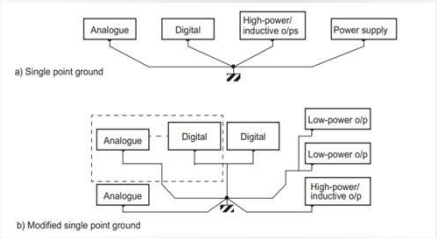
Current through the ground impedance

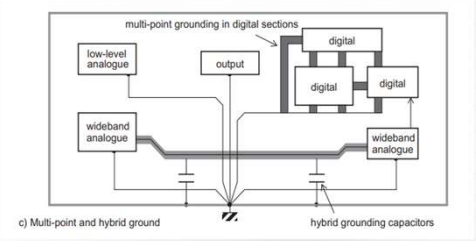
noise voltages along ground plane



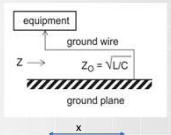
transimpedance





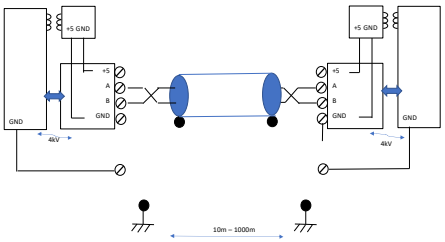


Ground (earth) cabel impedance

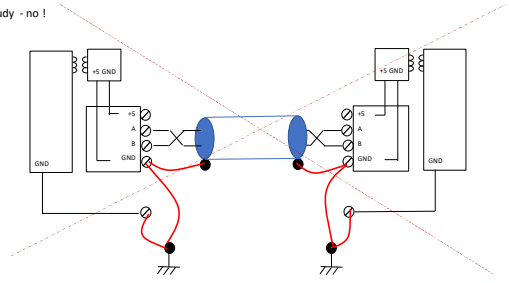


$$Z = Z_0 \tan\left(x \cdot \omega \sqrt{l/C}\right)$$

Case study ?

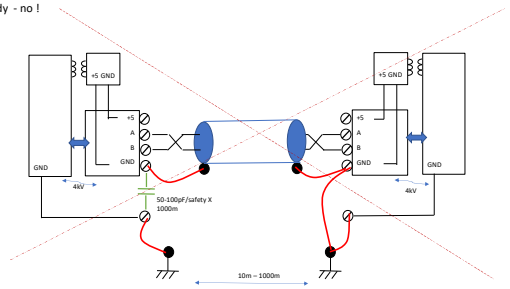


Case study - no !



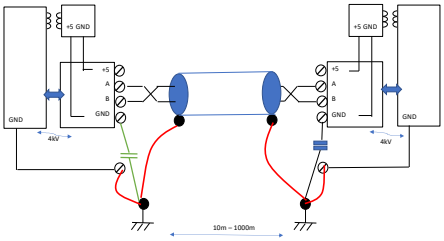
Not correct

Case study - no !



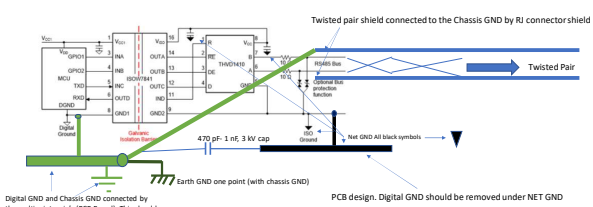
Not correct

Case study - yes !!!!



Correct

file:///C:/Users/jozef/Desktop/Sowa/TI%20APP%20Note/Top%207%20design%20questions%20about%20isolated%20RS-485%20transceivers%20-%20Analog%20-%20Technical%20articles%20-%20TI%20E2E%20support



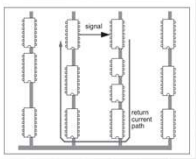
This concept I have used the last 20 years and never failed (Am I lucky???)

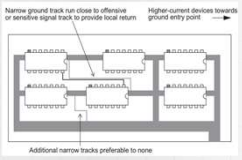
Single point – up to 1MHz

High frequencies – multipoint to low inductance ground plane or shield

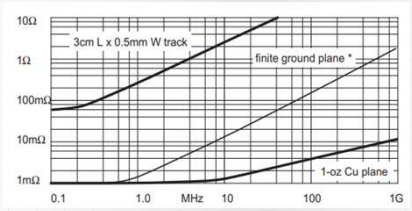
Shilded cabel with low transimpedance

Pcb layout





Track vs. plane impedance



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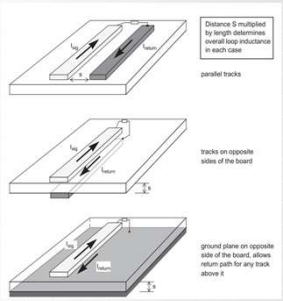
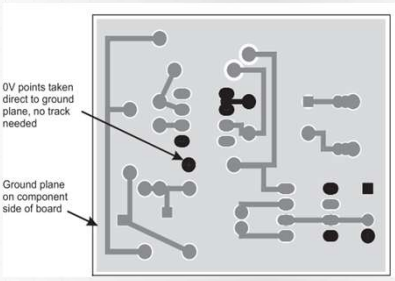


Impedance

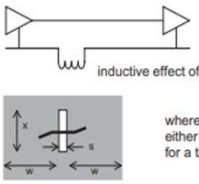
Low impedance (inductance)

23



24

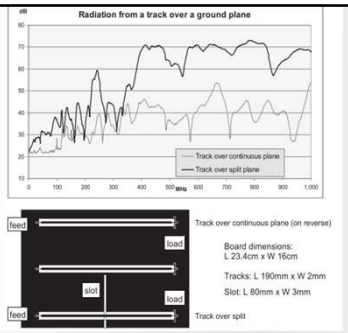
Avoid breaks in the ground plane



inductive effect of slot: $L = \frac{5 \cdot x}{2 + \ln(w/s)}$ nH

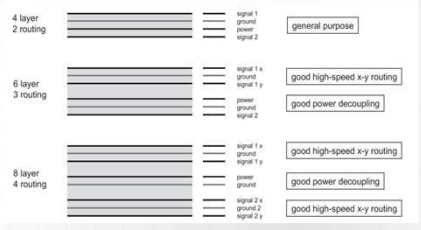
where x is the length of the slot in cm, w is the width of the plane either side of the slot, s is the width of the slot, w >> s and x << λ; for a track across the centre of the slot, w being equal either side

25



26

Multilayer boards



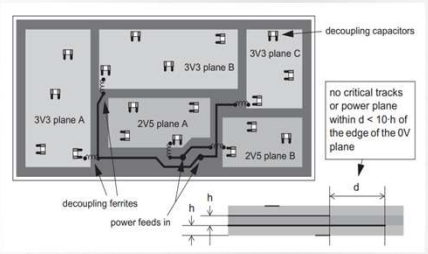
27

Grounding principles:
All conductors have a finite impedance which increases with frequency

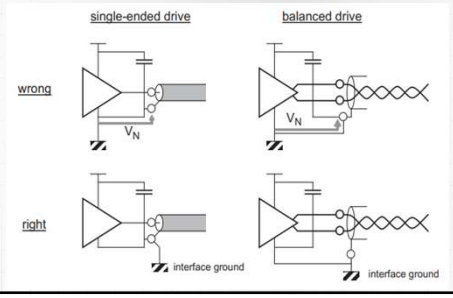
Two physically separate ground points are not at the same potential because current flows between them

At high frequencies there is no such thing as a single point ground because the stry capacitance

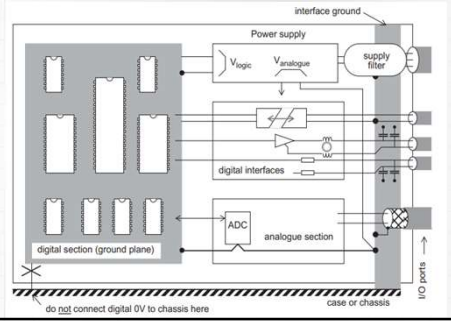
Power plane segmentation and the 10 · h rule



Screened cable connection



Separated grounds



31

Before routing begins:
- identify and label high di/dt circuits
- identify and label sensitive circuits
- identify 0V plane(s), including separate areas if these are vital
- identify power plane segments
- identify the interface ground plane
- decide on layer stack-up:
  - identify 0V plane layers
  - identify constant impedance layer(s)
  - identify power plane layer(s), next to 0V plane: some of these may also carry tracks in areas where power planes aren't needed
- check component placement to ensure:
  - no unnecessarily long track routes
  - no proximity of noisy components to sensitive ones
  - critical circuits away from ground plane edge – maximum partitioning of interfaces and functional sections: no unprotected interface routes to pass close to operational circuits
  - all filter components at the interface they are protecting, no functional circuits between the interface and the protection
- board-to-board connections: ground pins should be distributed along multi-way connectors close to high-speed or sensitive signals
- identify points for bonding the ground plane(s) to chassis

32

During routing:
- flag any breaks or gaps in a 0V plane and decide whether they are necessary or can be avoided
- ensure no tracks cross any unavoidable breaks in a 0V plane – if they must, then make sure series buffer resistors are placed appropriately at the break
- check that critical and constant-impedance tracks do not swap layers – if they must, they should be routed above or below a single 0V plane, not jump to a different 0V plane
- check adequate placement of decoupling capacitors – near device power pins – minimum inductance track/via layout
- ensure that interface filtering and transient protection is tracked with low inductance to the interface ground plane
- identify and control common impedance current paths for power switching circuits and sensitive wideband circuits
- check implementation of 10 · h rule for power planes and critical tracks versus the ground plane edge
- for balanced differential signal track pairs, confirm that adequate balance is maintained along the entire run – separation of at least 3 · h from other tracks is usually enough
- minimize surface areas of nodes with high dv/dt
- if empty areas of any layer are flood filled with copper, ensure that each such area is connected to 0V, not floating If you have to design a PCB without a 0V plane,
- identify critical (high-current, high di/dt or sensitive) circuit loops, including the appropriate segment of the 0V track
- minimize enclosed loop areas in these loops
- flood-fill and mesh the 0V tracks as much as possible

33

PCB high power

Institute for Interconnecting and Packaging Electronic Circuits (IPC)

IPC to **międzynarodowa organizacja non-profit**, która opracowuje **standardy techniczne** dla przemysłu elektronicznego, w szczególności dotyczące:
- projektowania płytek drukowanych (PCB),
- montażu komponentów elektronicznych,
- kontroli jakości i niezawodności produktów elektronicznych,
- materiałów i procesów produkcyjnych.

Główne serie norm IPC:
- **IPC-2221** – projektowanie PCB,
- **IPC-A-600** – akceptacja wykonania płytek PCB,
- **IPC-A-610** – akceptacja montażu elektronicznego,
- **IPC-7351** – projektowanie footprintów komponentów,
- **IPC-6012** – wymagania dla produkcji płytek.

EN IEC 61188

- Circuit boards and circuit board assemblies – Design and use

3. Dystans izolacyjny (clearance/creepage)

•Wysokie napięcia = odpowiednie odstępy między ścieżkami:

- 230 V AC → **min. 3 mm** (w powietrzu),
- 400 V i więcej → nawet **>6 mm**,
- użycie nacięć (slotów) w laminacie zwiększa efektywną drogę upływu.

•Warto zapoznać się z normą **IEC-60950 / IEC-62368 / IPC-2221**.

⚠ **1. Podstawowe napięcia sieciowe i wymagane odstępy (clearance):**

Napięcie (RMS)	Minimalny odstęp w powietrzu (clearance)	Uwagi
230 V AC	>**3 mm** (typowo 4 mm)	Dla podstawowej izolacji
400 V AC	>**6 mm**	Wymagana większa odległość
600 V+	**8 mm i więcej**	Wysokie napięcia, szczególna ostrożność

Źródło: **Norma IPC-2221** oraz **IEC-60950 / IEC-62368** (w zależności od zastosowania).

IPC 2221

Table 6-1 Electrical Conductor Spacing

Voltage Between Conductors (DC or AC Peaks)	Minimum Spacing						
	Bare Board				Assembly		
	B1	B2	B3	B4	A5	A6	A7
0-15	0.05 mm [0.00197 in]	0.1 mm [0.0039 in]	0.1 mm [0.0039 in]	0.05 mm [0.00197 in]	0.13 mm [0.00512 in]	0.13 mm [0.00512 in]	0.13 mm [0.00512 in]
16-30	0.05 mm [0.00197 in]	0.1 mm [0.0039 in]	0.1 mm [0.0039 in]	0.05 mm [0.00197 in]	0.13 mm [0.00512 in]	0.25 mm [0.00984 in]	0.13 mm [0.00512 in]
31-50	0.1 mm [0.0039 in]	0.6 mm [0.024 in]	0.6 mm [0.024 in]	0.13 mm [0.00512 in]	0.13 mm [0.00512 in]	0.4 mm [0.016 in]	0.13 mm [0.00512 in]
51-100	0.1 mm [0.0039 in]	0.6 mm [0.024 in]	1.5 mm [0.0591 in]	0.13 mm [0.00512 in]	0.13 mm [0.00512 in]	0.5 mm [0.020 in]	0.13 mm [0.00512 in]
101-150	0.2 mm [0.0079 in]	0.6 mm [0.024 in]	3.2 mm [0.126 in]	0.4 mm [0.016 in]	0.4 mm [0.016 in]	0.8 mm [0.031 in]	0.4 mm [0.016 in]
151-170	0.2 mm [0.0079 in]	1.25 mm [0.0492 in]	3.2 mm [0.126 in]	0.4 mm [0.016 in]	0.4 mm [0.016 in]	0.8 mm [0.031 in]	0.4 mm [0.016 in]
171-250	0.2 mm [0.0079 in]	1.25 mm [0.0492 in]	6.4 mm [0.252 in]	0.4 mm [0.016 in]	0.4 mm [0.016 in]	0.8 mm [0.031 in]	0.4 mm [0.016 in]
251-300	0.2 mm [0.0079 in]	1.25 mm [0.0492 in]	12.5 mm [0.4921 in]	0.4 mm [0.016 in]	0.4 mm [0.016 in]	0.8 mm [0.031 in]	0.8 mm [0.031 in]
301-500	0.25 mm [0.00984 in]	2.5 mm [0.0984 in]	12.5 mm [0.4921 in]	0.8 mm [0.031 in]	0.8 mm [0.031 in]	1.5 mm [0.0591 in]	0.8 mm [0.031 in]
> 500 See para. 6.3 for calc.	0.0025 mm /volt	0.005 mm /volt	0.025 mm /volt	0.00305 mm /volt	0.00305 mm /volt	0.00305 mm /volt	0.00305 mm /volt

B1 - Internal Conductors
B2 - External Conductors, uncoated, sea level to 3050 m [10,007 feet]
B3 - External Conductors, uncoated, over 3050 m [10,007 feet]
B4 - External Conductors, with permanent polymer coating (any elevation)
A5 - External Conductors, with conformal coating over assembly (any elevation)
A6 - External Component lead/termination, uncoated, sea level to 3050 m [10,007 feet]
A7 - External Component lead termination, with conformal coating (any elevation)

✎ **Typowe wartości z normy IPC-2221A (Tabela 6-1):**

Napięcie (DC lub AC RMS)	Minimalny odstęp (clearance) [mm]
30 V	0,13 mm
60 V	0,64 mm
120 V	1,0 mm
250 V	2,5 mm
500 V	5,0 mm
1000 V	10,0 mm
3000 V	22,0 mm

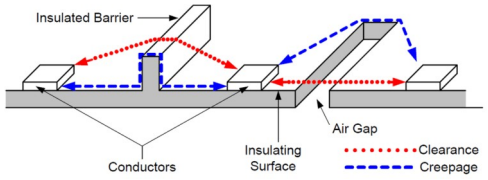
lakier

📌 **Czy IPC-2221 uwzględnia lakierowanie?**

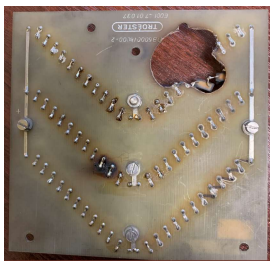
Nie bezpośrednio.

Norma IPC-2221 zakłada **gołą płytkę (bare board)** bez pokrycia. Jeśli stosujesz lakier (np. **conformal coating**), możesz **zmniejszyć wymagane odstępy, ale tylko wtedy**, gdy spełniasz dodatkowe wymagania określone w innych normach, np.:

- **IEC 60664-1** – mówi o odstępach dla napięć przy określonej **klasie zanieczyszczeń** i **typie izolacji** (czy to jest np. lakier, potting, powietrze itp.).
- **UL 94 / UL 746** – normy dla palności i wytrzymałości materiałów izolacyjnych (lakieru).



3ph rectifier hv practice



Maximum current of track

$$I = k(\Delta T)^{0.44} A^{0.725}$$

$$k = \begin{cases} 0.048 \text{ (external layers)} \\ 0.024 \text{ (internal layers)} \end{cases}$$

https://resources.altium.com/pl/p/ipc-2221-calculator-pcb-trace-current-and-heating#ipc-2221-trace-width-calculator

Grubość miedzi	Mikrometry (µm)	Milimetry (mm)	Uwagi
0.5 oz/ft²	~17 µm	0.017 mm	Cienka warstwa, stosowana przy precyzyjnych układach
1 oz/ft²	~35 µm	0.035 mm	Najczęściej stosowana grubość
2 oz/ft²	~70 µm	0.070 mm	Do wyższych prądów i mocy
3+ oz/ft²	105 µm i więcej	0.105 mm+	Grube ścieżki, np. w zasilaczach mocy

Jeśli nie jest podane inaczej, **standardowa grubość miedzi to 35 µm (1 oz/ft²)**.

Czy potrzebujesz tych danych do konkretnego projektu PCB?

Test problems

- List the rules for “system partitioning.”
- What is the mechanism of coupling distortions through common grounding?
- What is the difference between GROUNDING and EARTHING ?
- What is the difference between creepage and clearance?