

Wrocław University of Science and Technology

Analogue signals acquisition

WUT

Wrocław University of Science and Technology

References

- U. Tietze, Ch.Schenk, Electronics Circuits – Handbook for Design and Applications, Springer, 2010
- Advertisement materials and Application notes of:
 - Linear Technology,
 - Analog Device,
 - Texas Instruments,
 - National Semiconductors
 - NEV Corporation

Wrocław University of Science and Technology

Outline

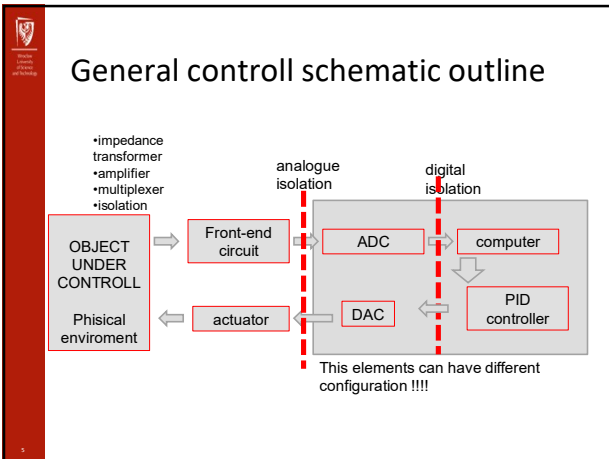
- Acquisition system –general diagram
- ADC – general information
- Isolation methods
- Multiplexing problems
- Sample & hold – sampling frequency
- Widowing

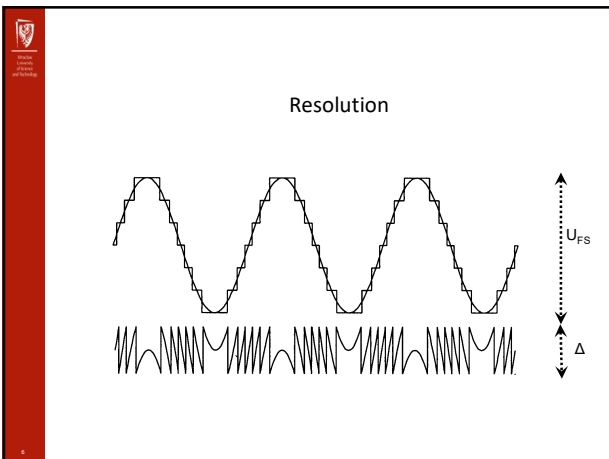
Introduction

The intent of this and a few next lectures is to introduce the students to the most commonly used transducer interfaces and to provide practical information for dealing with the most frequently encountered transducers and their associated signals.

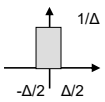
Transducers are available for measuring many physical quantities, such as temperature, pressure, strain, vibration, sound, humidity, flow, level, velocity, charge, pH, and chemical composition, among others. In most cases, the transducer manufacturer provides application notes on the transducer's use and principles of operation. The main questions to consider when selecting a transducer are:

- the electrical characteristics - source impedance, amplitude, frequency,
- power supply or excitation
- transducer's accuracy (taking frequency and range into account)
- calibration method
- verification of calibration
- environment of operation (temperature, humidity, vibration, pressure, etc.)





ADC – resolution and SNR



$$P_N = \int_{-\infty}^{\infty} x^2 p(x) dx = \frac{1}{\Delta} \int_{-\Delta/2}^{\Delta/2} x^2 dx = \frac{\Delta^2}{12} = \frac{(U_{FS}/2^n)^2}{12}$$

$$SNR = 10 \log \frac{P_S}{P_N} = 10 \log \left(\frac{(U_{FS}/2)^2}{\frac{(U_{FS}/2^n)^2}{12}} \right) = 6,02 \cdot n + 1,76 \text{ [dB]}$$

ADC ----SNR

$$SNR = 10 \log \frac{P_S}{P_N} = 10 \log \left(\frac{(U_{FS}/2)^2}{\frac{(U_{FS}/2^n)^2}{12}} \right) = 6,02 \cdot n + 1,76 \text{ [dB]}$$

$SNR = 20 \log 2 = 6,02 \text{ [dB]}$

For every bit of resolution SNR increases by 6dB !!!!!!!

For every bit of resolution, SNR increases by 6dB

!!!!!!!!!!

Channel Capacity [bit / second]

$$CC[\text{bits/sec}] = f_{\text{sample}} n_{\text{bits}} = 2B \log_2 \left(\frac{U_{FS}}{\Delta U} \right) =$$

$$= 2B \frac{\log_{10} \left(\frac{U_{FS}}{\Delta U} \right)}{\log_{10}(2)} = 2B \frac{\left\{ 20 \log_{10} \left(\frac{U_{FS}}{\Delta U} \right) \right\}}{20 \log_{10}(2)} = B \frac{SNR}{10 \log_{10}(2)} = \frac{B \cdot SNR}{3}$$

$$CC = \frac{B \cdot SNR}{3} [\text{bits/sec}]$$

Shannon-Hartley theorem

ADC Analog to Digital Converters

- parallel converter – flash
- successive approximation
- pipeline
- voltage to frequency
- integrating converter (two, four slop)
- delta-sigma converter

ADC – parallel (flash)

2-step converter
(direct, serial, pipeline)

Features (compared to „flash“):

- lower number comparators
- higher conversion time
- more popular (cheaper)
- higher resolution

13

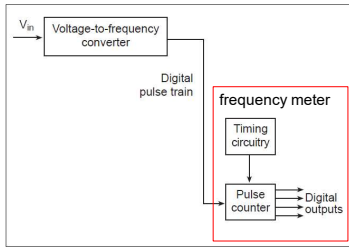
3-step converter
(direct, serial, pipeline)

14

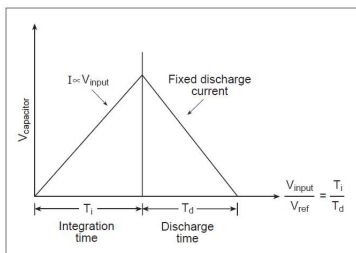
ADC - successive approximation

15

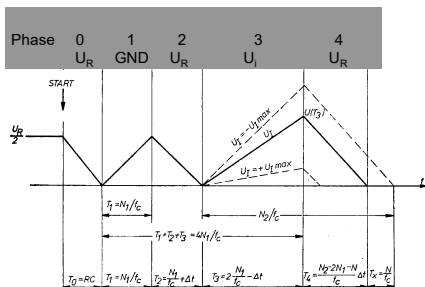
ADC - voltage to frequency

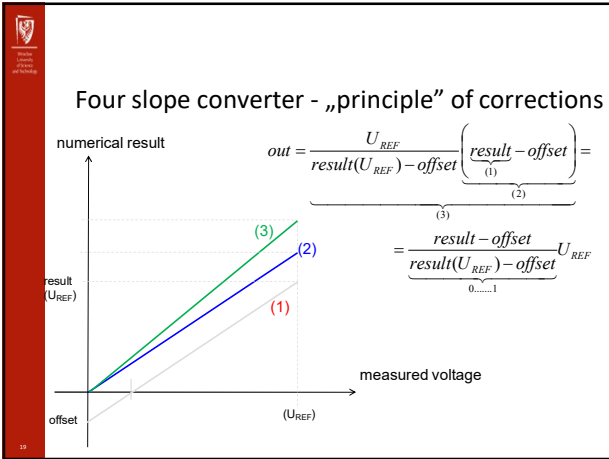


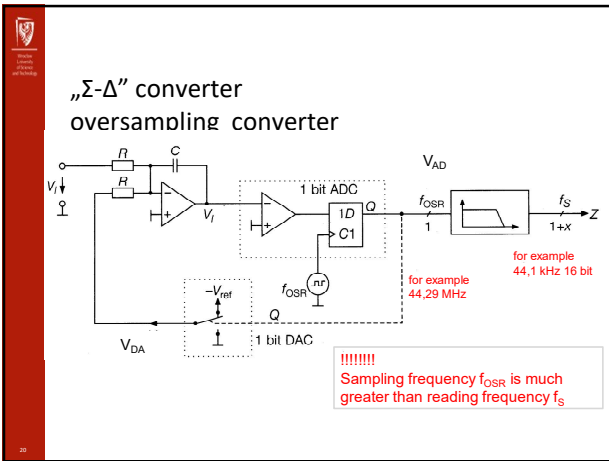
ADC - integrating converter

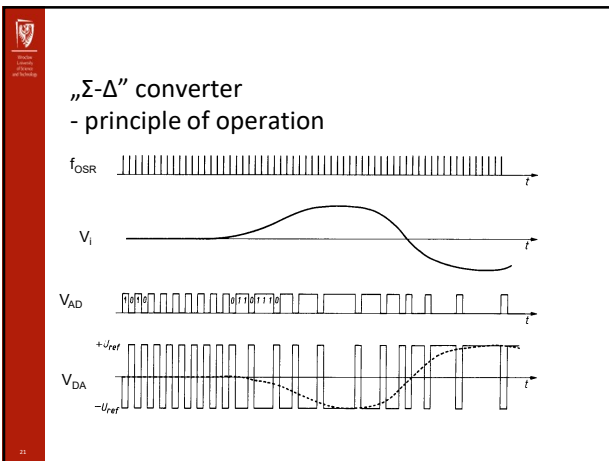


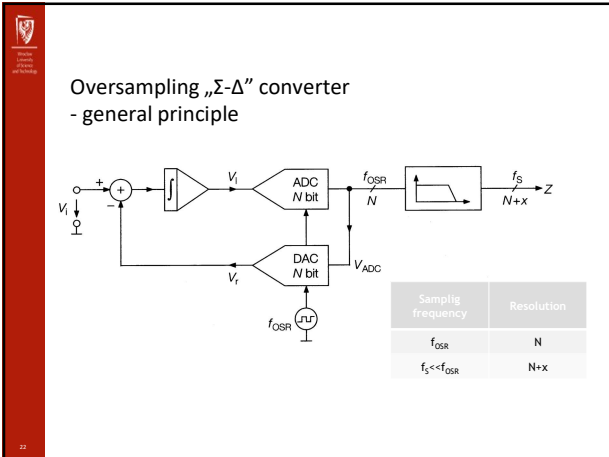
Indirect converter ---four - slope

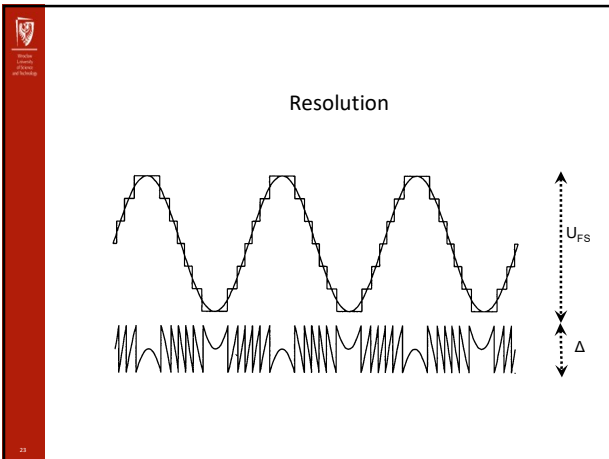












ADC – resolution and SNR

$$P_N = \int_{-\infty}^{\infty} x^2 p(x) dx = \frac{1}{\Delta} \int_{-\Delta/2}^{\Delta/2} x^2 dx = \frac{\Delta^2}{12} = \frac{\left(\frac{U_{FS}}{2^n}\right)^2}{12}$$

$$SNR = 10 \log \frac{P_S}{P_N} = 10 \log \left(\frac{\left(\frac{U_{FS}}{2}\right)^2}{\frac{\left(\frac{U_{FS}}{2^n}\right)^2}{12}} \right) = 6,02 \cdot n + 1,76 \text{ [dB]}$$

21

Noise shaping in „Σ-Δ” converter

The diagram shows three scenarios for quantization noise spectrum:

- A Nyquist Operation:** The noise spectrum is a flat rectangular pulse from $f_s/2$ to f_s . The area is labeled "QUANTIZATION NOISE = $q^2/12$, $q = 1 \text{ LSB}$ ".
- B Oversampling + Digital Filter + Decimation:** The noise spectrum is a flat rectangular pulse from $f_s/2$ to $Kf_s/2$. A "DIGITAL FILTER" is shown removing noise between $f_s/2$ and f_s . The remaining noise is between f_s and $Kf_s/2$.
- C Oversampling + Noise Shaping + Digital Filter + Decimation:** The noise spectrum is a triangular pulse peaking at $f_s/2$ and reaching zero at $Kf_s/2$. A "DIGITAL FILTER" is shown removing noise between $f_s/2$ and f_s . The remaining noise is between f_s and $Kf_s/2$.

22

„Σ-Δ” converter – linear model

The linear model consists of a summing junction Σ where the input X is added and the output Y is subtracted. The result $X - Y$ passes through an "ANALOG FILTER" with transfer function $H(f) = \frac{1}{f}$. The output of the filter is then summed with "Q = QUANTIZATION NOISE" to produce the final output Y .

$$Y = \frac{1}{f}(X - Y) + Q$$

REARRANGING, SOLVING FOR Y:

$$Y = \frac{X}{f+1} + \frac{Qf}{f+1}$$

The first term is labeled "SIGNAL TERM" and the second term is labeled "NOISE TERM".

23

Conventional ADC: Shows a spectrum with a narrow "Desired Input Spectrum" (green) and "Frequencies to be Rejected" (red) concentrated near the "Sampling Frequency".

Delta Sigma ADC: Shows a spectrum with a narrow "Desired Input Spectrum" (green) and "Frequencies Rejected by Design" (yellow) spread across the frequency range up to the "Sampling Frequency". "Frequencies to be Rejected" (red) are concentrated near the "Sampling Frequency".

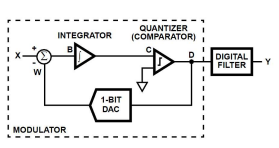
Conventional converter

$$U_{Nout} \propto \frac{1}{\sqrt{f_{os}/f_s}}$$

$$N_{bits} = \frac{20 \log \sqrt{f_{os}/f_s}}{6dB/bit}$$

f_{os}/f_s	bit
2	0.5
4	1
256	4

First order „Δ-Σ” converter

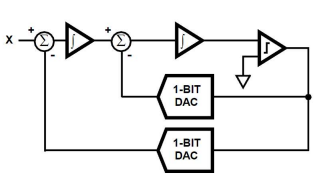


$$U_{Nout} \propto \left(\frac{1}{\sqrt{f_{os}/f_s}} \right)^3$$

$$N_{bits} = \frac{20 \log \left(\sqrt{f_{os}/f_s} \right)^3}{6dB/bit}$$

f_{os}/f_s	bit
2	1.5
4	3
256	12

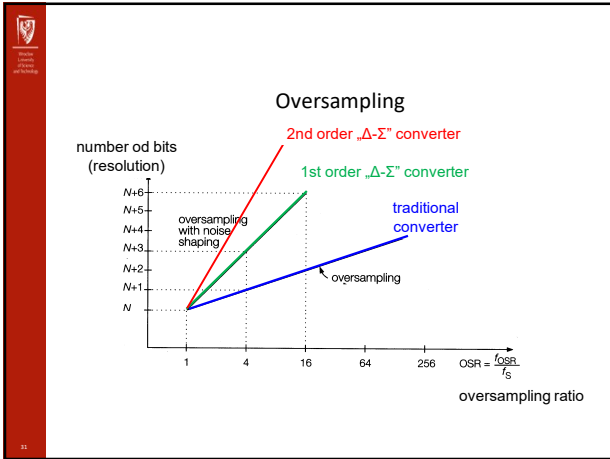
2nd order „Δ-Σ” converter

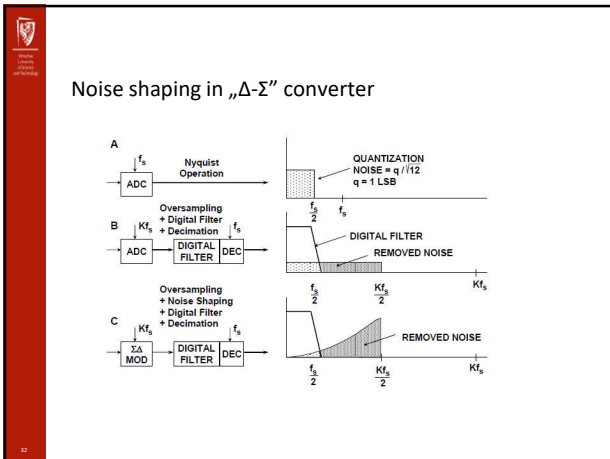


$$U_{Nout} \propto \left(\frac{1}{\sqrt{f_{os}/f_s}} \right)^5$$

$$N_{bits} = \frac{20 \log \left(\sqrt{f_{os}/f_s} \right)^5}{6dB/bit}$$

f_{os}/f_s	bit
2	2.5
4	5
256	20





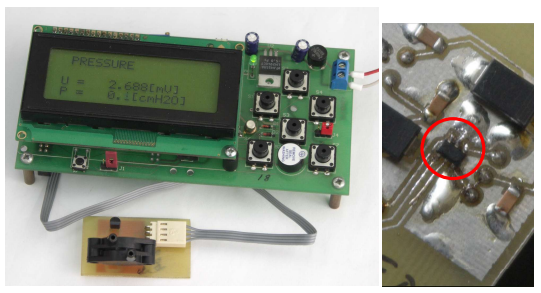
**Example of „ Δ - Σ ” converter
ADS1110**

FEATURES

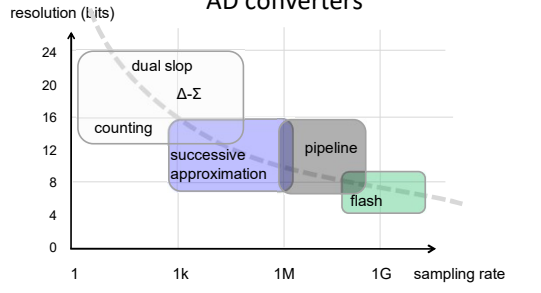
- COMPLETE DATA ACQUISITION SYSTEM IN A TINY SOT23-8 PACKAGE
- ONBOARD REFERENCE: Accuracy: 2.045V \pm 0.05%; Drift: 5ppm/°C
- ONBOARD PGA
- ONBOARD OSCILLATOR
- 16-BITS NO MISSING CODES
- INL: 0.01% of FSR max
- CONTINUOUS SELF-CALIBRATION
- SINGLE-CYCLE CONVERSION
- PROGRAMMABLE DATA RATE: 15SPS TO 240SPS
- I²C™ INTERFACE—EIGHT AVAILABLE ADDRESSES
- POWER SUPPLY: 2.7V to 5.5V
- LOW CURRENT CONSUMPTION: 240 μ A

The block diagram shows the internal components of the ADS1110: a 2.045V reference, a PGA, an Δ - Σ converter, an I²C interface, and a clock oscillator. The pinout diagram shows the 8 pins of the SOT23-8 package: 1 (GND), 2 (V_{DD}), 3 (V_{REF}), 4 (V_{IN}), 5 (V_{IN}), 6 (SCL), 7 (SDA), and 8 (GND).

Lab setup of pressure sensor

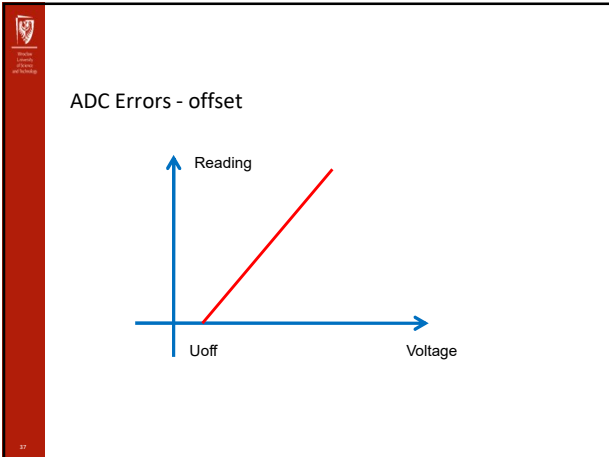


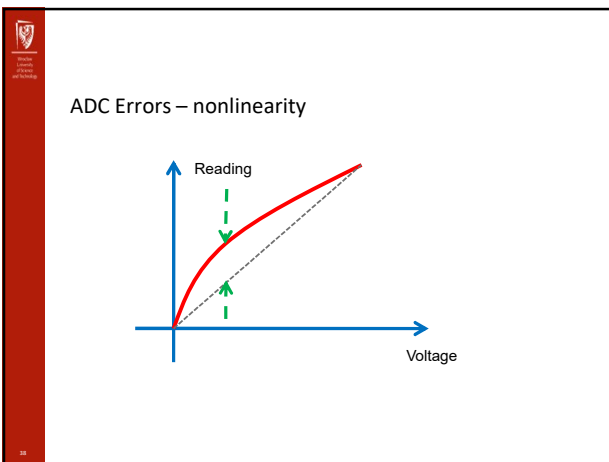
General comparison of AD converters

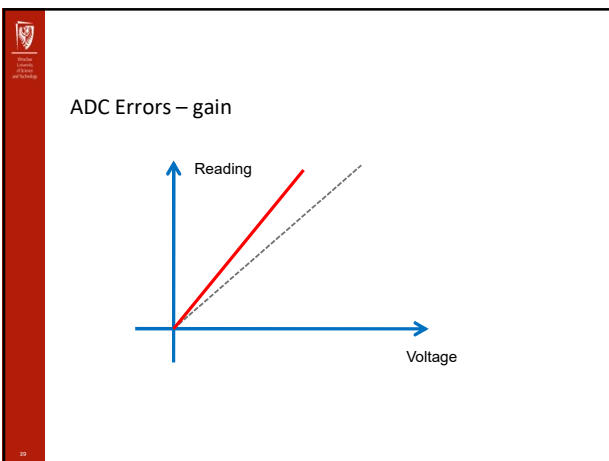


ADC Errors

- offset
- linearity
- gain
- missing codes
- noise (interferences)







ADC Errors – missing codes

40

ADC Errors - noise (interferences)

Controlling noise is first step to measure anything.

Spending money for accurate and high resolution ADC can be worthless when measuring signal is interfered by high level noise.

noise level should be smaller than resolution

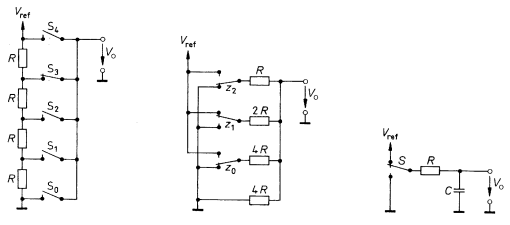
41

Digital to analog conversion

42



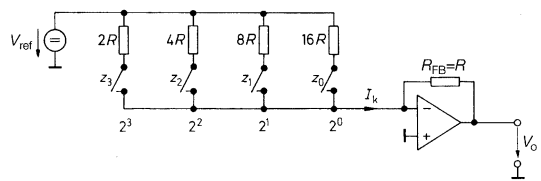
Digital to Analogue Conversion



the parallel method the weighting method computing method



Weighting conversion

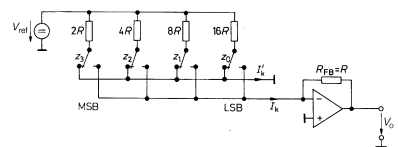


$$U_{out} = -U_{ref} \frac{N}{N_{max} + 1}$$

TIP:
 difficult for manufacturing because of different R;
 U_{ref} is loaded depending N;
 stray capacitance of switches are charged or dis- every change;



Weighting conversion



TIP:
 difficult for manufacturing because of different R;
 U_{ref} is loaded depending N;
 stray capacitance of switches are charged or dis- every change;

Ladder network

TIP:
difficult for manufacturing because of different R;
 U_{ref} is loaded depending on N;
stray capacitance of switches are charged or discharged every change;

$$U_{out} = -U_{ref} \frac{N}{N_{max} + 1}$$

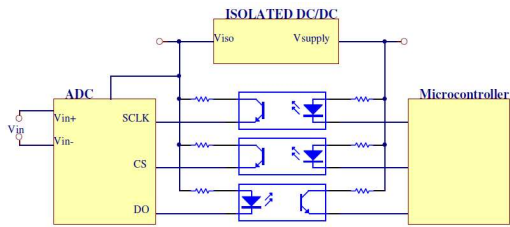
Ladder network converter without any amp

Isolation

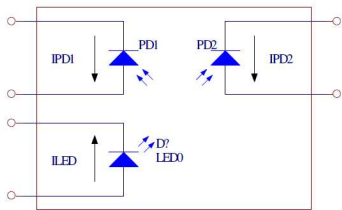
- Optical
- Magnetic
- Capacitive

- Analogue
- Digital

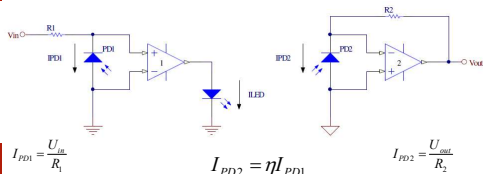
„Digitally“ isolatet analog signals



Opto-Isolation of analog signals



Analog opto-isolation



$$I_{PD1} = \frac{U_{in}}{R_1}$$

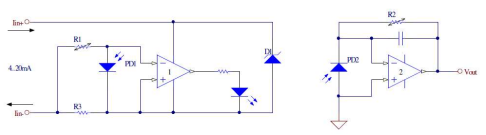
$$I_{PD2} = \eta I_{PD1}$$

$$I_{PD2} = \frac{U_{out}}{R_2}$$

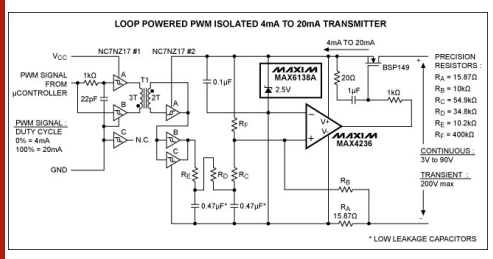
$$U_{out} = U_{in} \frac{R_2}{R_1} \eta$$

Tip: accuracy can be is not satisfactory

Opto-isolation of 4-20mA loop

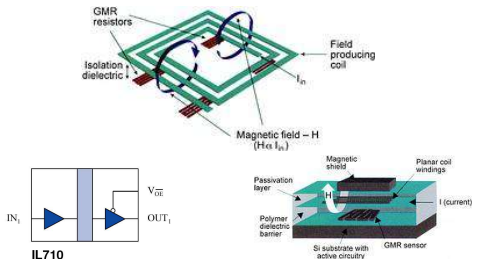


PWM to 4-20mA isolation

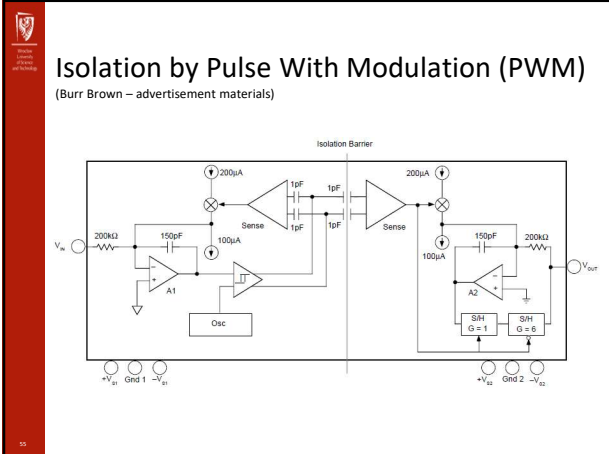


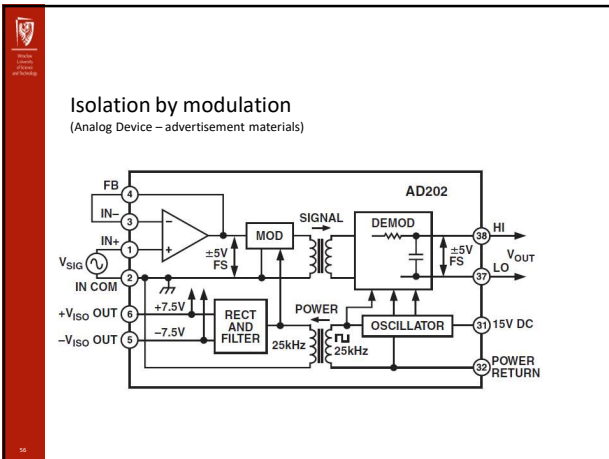
MAXIM only advertisement materials

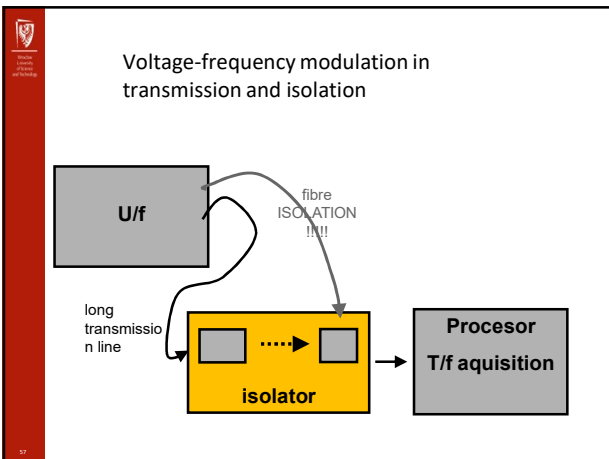
Magneto - Isolation



NVE corporation
Advertisement materials



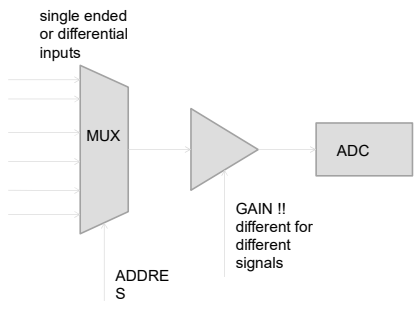




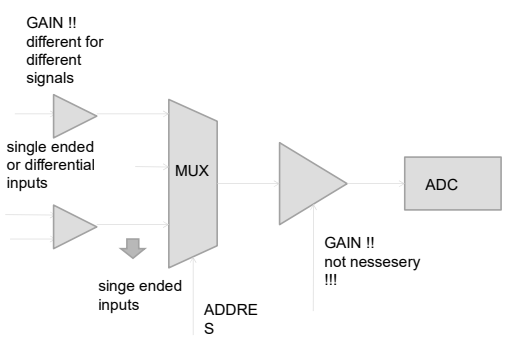
Multiplexing

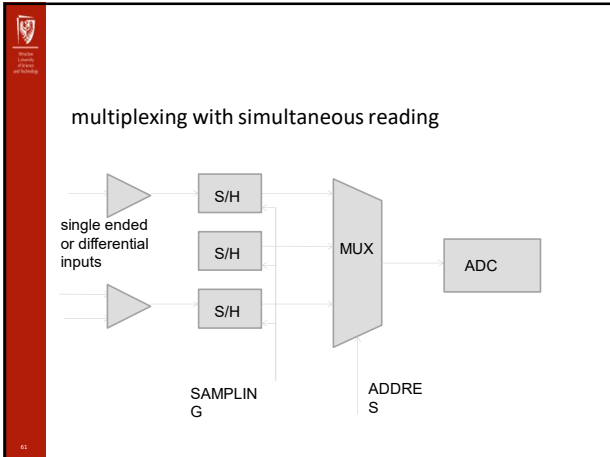
- direct (small signal) multiplexing
- buffering – multiplexing
- simultaneous s/h
- digital multiplexing

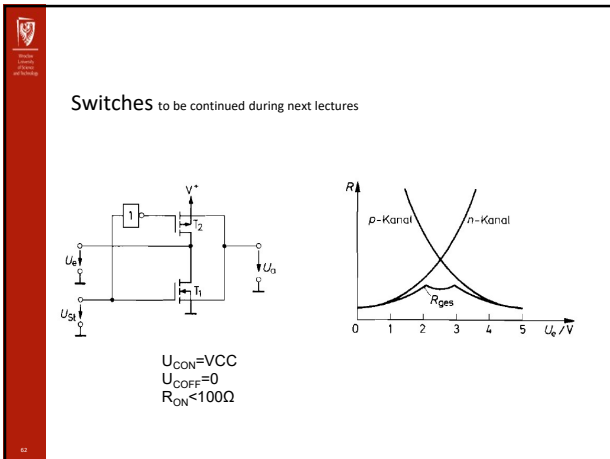
direct multiplexing



Input buffering







MOSFET switches overview

Type	Manufacturer	Function	On resistance	Voltage range	Power dissipation	Response time
Without level translator, unprotected						
74 HC 4016	Philips	4 × SPST	65 Ω	0...12 V	10 μW	10 ns
74 HC 4053	Philips	3 × SPDT	60 Ω	0...12 V	10 μW	20 ns
74 HC 4066	Philips	4 × SPST	35 Ω	0...12 V	10 μW	20 ns
MAX 4522	Maxim	4 × SPST	60 Ω	0...12 V	10 μW	10 ns
SD 5000	Vishay	4 × SPST	30 Ω	± 10 V	10 μW	1 ns
Fast switching (≤ 100 ns)						
HI 201 HS	Intersil	4 × SPST	30 Ω	± 15 V	120 mW	30 ns
74 HC 4316	Philips	4 × SPST	65 Ω	± 5 V	10 μW	20 ns
DG 611	Vishay	4 × SPST	18 Ω	± 5 V	20 μW	15 ns
Low power (≤ 100 μW) and low on resistance (≤ 100 Ω)						
ADG 511	Analog D.	4 × SPST	30 Ω	± 20 V	20 μW	200 ns
DG 403	Intersil	2 × SPDT	30 Ω	± 15 V	20 μW	150 ns
DG 411	Intersil	4 × SPST	30 Ω	± 15 V	30 μW	150 ns
LT 221	Lin. Tech.	4 × SPST	70 Ω	± 15 V	10 μW	250 ns
MAX 351	Maxim	4 × SPST	22 Ω	± 15 V	35 μW	150 ns
DG 405	Vishay	4 × SPST	20 Ω	± 15 V	10 μW	100 ns

MOSFET switches overview cont.

Low on resistance ($\leq 100 \Omega$)						
ADG 211	Analog D.	4 × SPST	60 Ω	± 15 V	10 μ W	200 ns
ADG 333	Analog D.	4 × SPDT	20 Ω	± 15 V	1 μ W	150 ns
ADG 451	Analog D.	4 × SPST	5 Ω	± 15 V	20 μ W	60 ns
MAX 4602	Maxim	4 × SPST	2 Ω	± 15 V	1 μ W	180 ns
CDG 271	Vishay	4 × SPST	32 Ω	± 15 V	150 mW	50 ns
High voltage ($\geq \pm 30$ V)						
HV 348	Supertex	2 × SPST	35 Ω	± 50 V	10 mW	500 ns
High off attenuation (≥ 40 dB @ 100 MHz)						
HI 222	Intersil	2 × SPST	35 Ω	± 15 V	75 mW	90 ns
MAX 4545	Maxim	2 × SPST	50 Ω	± 5 V	1 μ W	100 ns
DG 540	Vishay	4 × SPST	30 Ω	± 6 V	60 mW	30 ns

Understanding switches description

SPST Single(Double)Pole

SPDT Single(Double;Triple)Thro
w

DPST

DPDT

SPCO – centere off

Analogue multiplexers

Type	Manu- facturer	Function	On resistance	Voltage range	Power dissipation	Response time	Data latch
Fast switching (≤ 100 ns), unprotected							
74 HC 4051	Philips	1 × 8	60 Ω	± 5 V	10 μ W	20 ns	no
74 HC 4052	Philips	2 × 4	60 Ω	± 5 V	10 μ W	20 ns	no
74 HC 4053	Philips	3 × 2	60 Ω	± 5 V	10 μ W	20 ns	no
Low power ($\leq 100 \mu$ W)							
DG 406	Maxim	1 × 16	80 Ω	± 15 V	20 μ W	300 ns	no
DG 408	Maxim	1 × 8	80 Ω	± 15 V	20 μ W	200 ns	no
DG 685	Vishay	1 × 8	55 Ω	± 15 V	10 μ W	160 ns	yes
High input protection ($\geq \pm 30$ V)							
MAX 378	Maxim	1 × 8	2 k Ω	± 15 V	2 mW	300 ns	no
DG 458	Intersil	1 × 8	80 Ω	± 15 V	5 mW	200 ns	no
High voltage ($\geq \pm 30$ V)							
HV 22816	Supertex	1 × 8	22 Ω	± 80 V	2 mW	4 μ s	yes

SH – sample and hold – basic circuit
to be continued during next lectures

$R_{out}=0$ $R_{in}=\infty$

Time acquisition channel

external settle time T_1 [ns-us] Settle time of ADC T_2 [ns-us]

$$T_{sample} \geq \sqrt{T_1^2 + T_2^2} = T_{settle} \quad f_{acq} = \frac{1}{N_{channel} \cdot T_{sample}}$$

Summary

- Acquisition system – general diagram
- ADC – general information
- isolation methods
- Multiplexing problems
- Sample & hold – sampling frequency



Test questions (an example):

- In digital to analog conversion, what is the signal to quantization noise ratio ?
- What is the relationship between SNR and Channel Capacity ?
- Describe relationship between sampling ratio and resolution of AD converters.
- What are basic principles (methods) of galvanic isolation in analog and digital systems ?

72



Multiplexers & switches – more about in „AD/DA converters lecture“

72



Windowing (facultative)

High- and moderate-resolution windows

- 1 Rectangular window
- 2 Hann window
- 3 Hamming window
- 4 Tukey window
- 5 Cosine window
- 6 Lanczos window
- 7 Triangular windows
- 8 Gaussian windows
- 9 Bartlett–Hann window
- 10 Blackman windows
- 11 Kaiser windows

72



Windowing

Low-resolution (high-dynamic-range) windows

1 Nuttall window, continuous first derivative

2 Blackman–Harris window

3 Blackman–Nuttall window

4 Flat top window

73



Windowing

Other windows

1 Bessel window

2 Dolph-Chebyshev window

3 Hann-Poisson window

4 Exponential or Poisson window

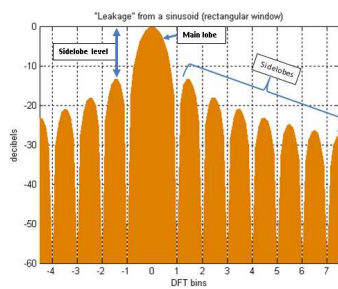
5 Rife-Vincent window

6 DPSS or Slepian window

74



Main and side lobes



75

