

Design checklist to assess your design against EMC.
TIP 6:

6. • Grounding:

- a) • design and enforce the ground system at the product definition stage
- b) • consider the ground system as a return current path, not just as 0V reference
- c) • provide for parallel earth conductors at the system level
- d) • ensure metal-to-metal bonding of screens, connectors, filters, and enclosure panels; ensure that bonding methods will not deteriorate in adverse environments
- e) • mask paint from, and apply a conductive finish to, any intended contact surfaces; keep earth straps short and define their geometry
- f) • avoid common ground impedances for different circuits; provide an interface ground area for decoupling and filtering

GROUNDING vs. EARTHING

grounding (USA)

give a reference potential (0V) for external connections to the system
a low impedance path by which current can return to its source

connection to the earth for safety purposes
Yellow-green cable

primary – ring road expedites traffic within town

secondary – traffic control encourages traffic to use bypass

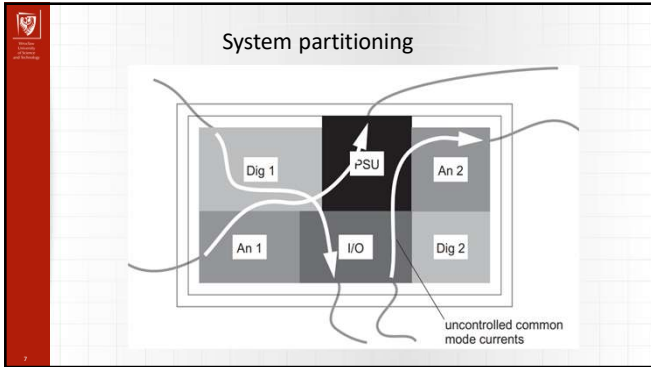
tertiary – bypass keeps traffic away from town centre

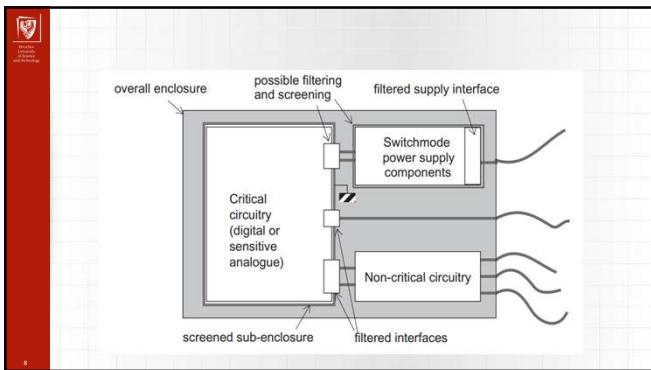
primary – circuit layout

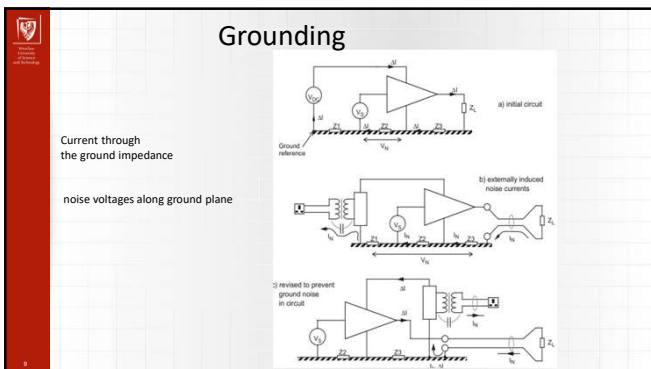
tertiary – shielding

secondary – interface filtering

Not only the 0V reference, but also the return current







transimpedance

increasing Z_T

$Z_T = R_G + j\omega(L_G - M)$
is a function of circuit and ground geometry

$V_{AVT} = I_{CM} \cdot Z_T$

$V_c = 0.5(V_G + V_{AVT})$
if $Z_S = Z_L \gg Z_T$

Labels in diagram: V_S , Z_S , signal circuit, mutual inductance M , R_G , L_G , ground structure, Z_L , V_{AVT} , V_c , I_{CM} .

a) Single point ground

b) Modified single point ground

multi-point grounding in digital sections

c) Multi-point and hybrid ground

hybrid grounding capacitors

Ground (earth) cable impedance

equipment

ground wire

$Z \rightarrow$

$Z_0 = \sqrt{L/C}$

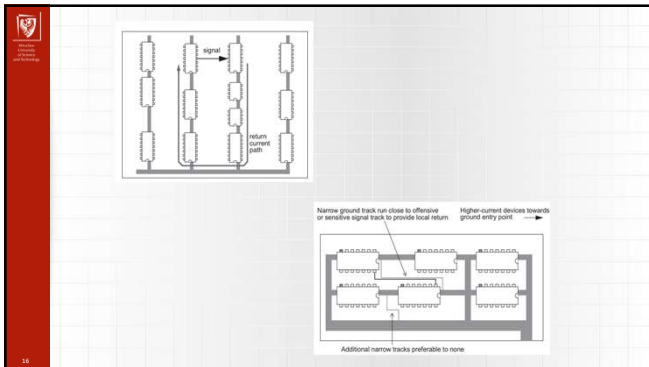
ground plane

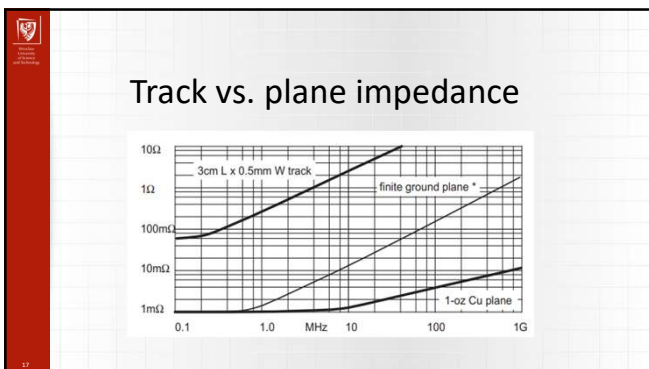
x

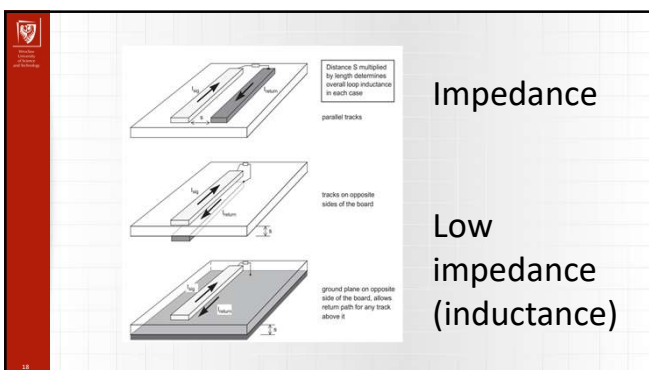
$Z = Z_0 \tan \left(x \cdot \omega \sqrt{L/C} \right)$

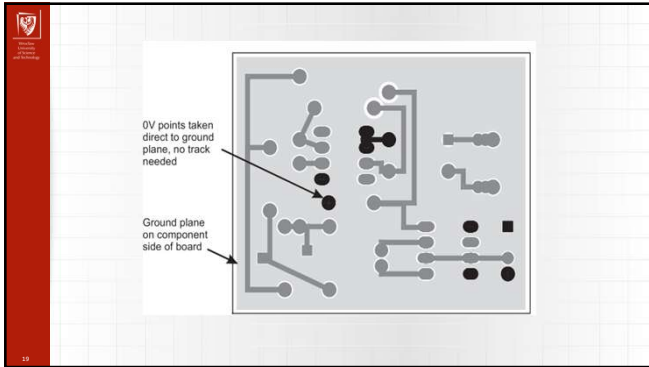
1. Single point – up to 1MHz
2. High frequencies – multipoint to low inductance ground plane or shield
Shielded cable with low transimpedance

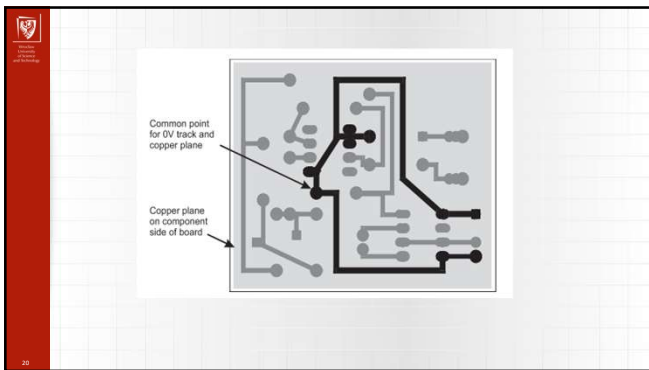
Pcb layout

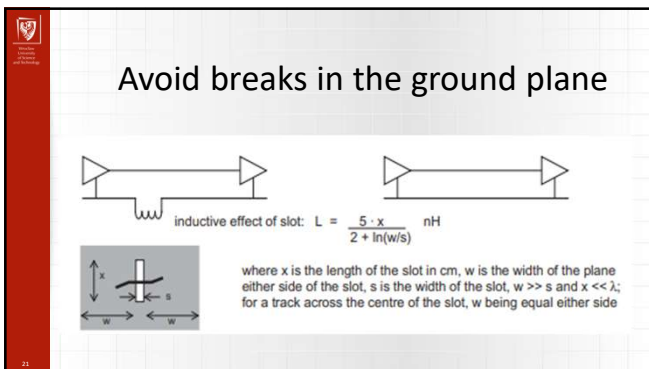


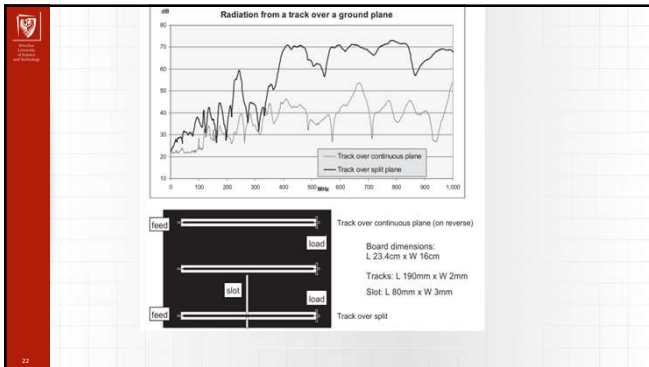


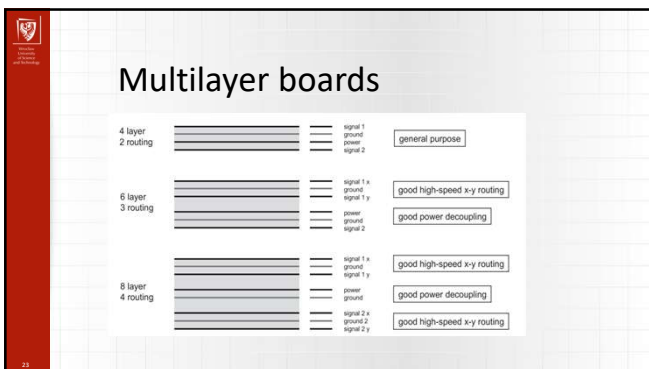












Grounding principles:
All conductors have a finite impedance which increases with frequency

Two physically separate ground points are not at the same potential because current flows between them

At high frequencies there is no such thing as a single point ground because the stray capacitance

Power plane segmentation and the 10 · h rule


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Screened cable connection

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Separated grounds

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 Before routing begins:

- identify and label high di/dt circuits
- identify and label sensitive circuits
- identify OV plane(s), including separate areas if these are vital
- identify power plane segments
- identify the interface ground plane
- decide on layer stack-up:
 - identify OV plane layers
 - identify constant impedance layer(s)
 - identify power plane layer(s), next to OV plane: some of these may also carry tracks in areas where power planes aren't needed
- check component placement to ensure:
 - no unnecessarily long track routes
 - no proximity of noisy components to sensitive ones
 - critical circuits away from ground plane edge – maximum partitioning of interfaces and functional sections: no unprotected interface routes to pass close to operational circuits
 - all filter components at the interface they are protecting, no functional circuits between the interface and the protection
- board-to-board connections: ground pins should be distributed along multi-way connectors close to high-speed or sensitive signals
- identify points for bonding the ground plane(s) to chassis

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 During routing:

- flag any breaks or gaps in a OV plane and decide whether they are necessary or can be avoided
- ensure no tracks cross any unavoidable breaks in a OV plane – if they must, then make sure series buffer resistors are placed appropriately at the break
- check that critical and constant-impedance tracks do not swap layers – if they must, they should be routed above or below a single OV plane, not jump to a different OV plane
- check adequate placement of decoupling capacitors – near device power pins – minimum inductance track/via layout
- ensure that interface filtering and transient protection is tracked with low inductance to the interface ground plane
- identify and control common impedance current paths for power switching circuits and sensitive wideband circuits
- check implementation of 10 - h rule for power planes and critical tracks versus the ground plane edge
- for balanced differential signal track pairs, confirm that adequate balance is maintained along the entire run – separation of at least 3 · h from other tracks is usually enough
- minimize surface areas of nodes with high dv/dt
- if empty areas of any layer are flood filled with copper, ensure that each such area is connected to OV, not floating

If you have to design a PCB without a OV plane,

- identify critical (high-current, high di/dt or sensitive) circuit loops, including the appropriate segment of the OV track
- minimize enclosed loop areas in these loops
- flood-fill and mesh the OV tracks as much as possible

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