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EMC basic aspects 2

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References

1. Williams T., *EMC for Product Designers*, Elsevier-Newnes, 5th ed., Oxford, 2015
2. Ott H. W., *Electromagnetic Compatibility Engineering*, Wiley, Hoboken, NJ, 2009

Ilustrations in this presentation are takem mostly from above

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ElectroMagnetic Sources in EM Environment

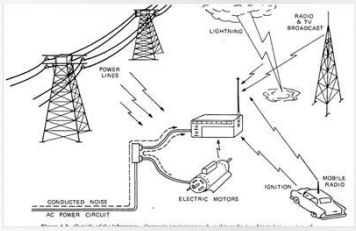

Fig. from: H.W.Ott *Noise Reduction Techniques in Electronic Systems*

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Electronic System as a Noise Source

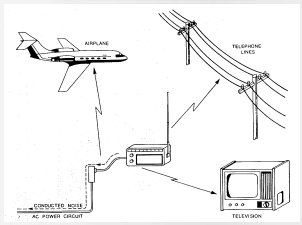

Fig. from: H.W.Ott *Noise Reduction Techniques in Electronic Systems*

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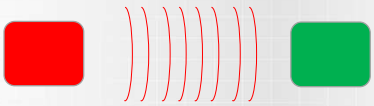
Radiated

emission / susceptibility



30MHz –1000MHz(more!)

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Conducted

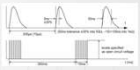
emission / susceptibility

(20Hz)150kHz – 30MHz

6

ESD & Lighting susceptibility

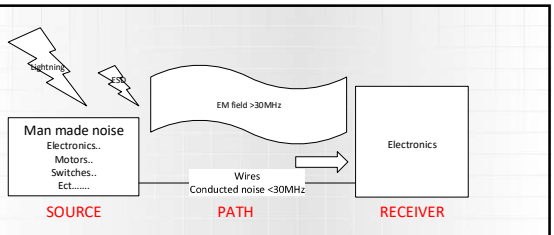
Electrical fast transient (EFT) bursts



Low frequency tests

Magnetic field 50(60)Hz

Current harmonics



3 elements of EMC trouble

SOURCE PATH RECEIVER

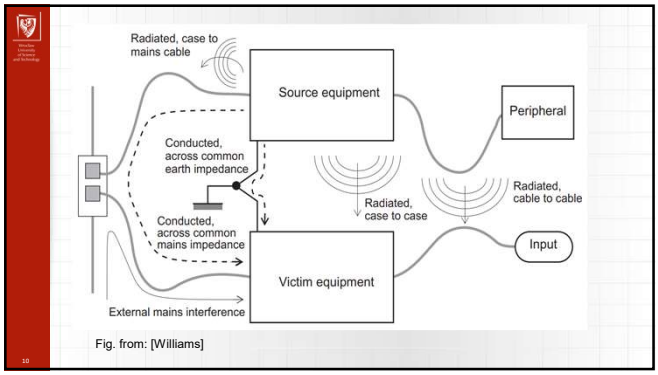


Fig. from: [Williams]

„Transmitters" and „Receivers"

- Transmitters (sources of disturbance)
  - car ignition systems
  - fluorescent lamps
  - universal motors
  - power supply units
  - switching contacts
  - atmospherical discharges
  - integrated circuit microprocessors
  - etc.
- Receiver
  - broadcasting and TV receivers
  - automation systems
  - microelectronics (e.g. cars, toys)
  - measuring instruments, controlling devices and instruments
  - data processing equipment (Computers)
  - heart pacemakers
  - bio-organisms
  - etc

Design checklist to assess your design against EMC:

1. • Design for EMC from the beginning; know what performance you require; During the design/prototyping process, perform "precompliance" testing
2. • Partition the system into critical and non-critical sections
   - a) • determine which circuits will be noisy or susceptible and which will not
   - b) • lay them out in separate areas as far as possible
   - c) • select internal and external interface locations to allow optimum common mode current control
3. • Select components and circuits with EMC in mind
   - a) • use or and/or high-immunity logic; apply slew rate limiting to data transmission interfaces
   - b) • use series R/I buffering on all high-speed clock and data lines
   - c) • use good power decoupling techniques: small, low-inductance capacitors adjacent to the ICs they are decoupling
   - d) • use series ferrite chips in the supplies to create power segments
   - e) • reduce fan-out on clock circuits by liberal use of buffers
   - f) • minimize analogue signal bandwidths
   - g) • maximize dynamic range of analogue signal paths
   - h) • check stability in wideband amplifiers
   - i) • don't leave unused IC input pins floating tie them to 0V or VCC
   - j) • include raw-side ferrite or capacitive filtering at all sensitive analogue inputs
   - k) • include raw-side ferrite or capacitive filtering at all sensitive analogue inputs
   - l) • avoid edge triggered digital inputs if possible, protect them if unavoidable
4. • PCB layout
   - a) • refer to separate checklist in section about PCB design
5. • Cables
   - a) • segregate, and avoid parallel runs of, signal and power cables
   - b) • choose RF-screened cables if the wanted signal cannot be properly filtered
   - c) • avoid screened cable with the screen connected only at one end; if unavoidable, treat the cable as unscreened at RF
   - d) • use twisted pair both within and outside an enclosure, for balanced or high-dI/dt lines
   - e) • use properly designed looms, ribbon or flex for internal wiring – avoid loose wires or bundles
   - f) • run cables away from apertures in the shielding, but close to conductive grounded structures
   - g) • apply ferrite suppressors to damp resonances and control common mode currents
   - h) • ensure that cable screens are properly terminated to the connector backshell; avoid pigtails
   - i) • terminate lines carrying high frequency signals with the correct transmission line impedance
6. • Grounding
   - a) • design and enforce the ground system at the product definition stage
   - b) • consider the ground system as a return current path, not just as 0V reference
   - c) • provide for parallel earth conductors at the system level
   - d) • ensure metal-to-metal bonding of screens, connectors, filters, and enclosure panels • ensure that bonding methods will not deteriorate in adverse environments
   - e) • mask paint from, and apply a conductive finish to, any intended contact surfaces • keep earth straps short and define their geometry
   - f) • avoid common ground impedances for different circuits • provide an interface ground area for decoupling and filtering
7. • Filters
   - a) • assume that a supply filter is needed; design the filter for the application
   - b) • filter all I/O lines, using either or both of three-terminal capacitors to interface ground, and common mode chokes
   - c) • apply π filters at the DC power input to each board, in multi-board designs
   - d) • ensure a defined ground return for each filter
   - e) • apply filtering to interference sources, such as switches or motors, directly at their terminals
   - f) • locate all filter components and associated wiring or tracks adjacent to the interface being filtered
8. • Shielding
   - a) • design all metallic structures as if they were electrical components: account for their stray capacitance and inductance
   - b) • consider segregated enclosures: enclose particularly sensitive or noisy areas with extra internal shielding
   - c) • avoid large or resonant apertures in a shield, or take measures to mitigate them
   - d) • avoid dipole-like structures in a metallic enclosure
   - e) • ensure that separate panels are well bonded along their seams using conductive gaskets: apply good bonding practice as in "grounding" above
   - f) • design plastic enclosures to allow internal conductive coating if necessary
   - g) • decide on and implement DC or RF tie points between circuit 0V and the shield
   - h) • use multiple internal tie-points to minimize box resonances
9. • During the design/prototyping process, perform "precompliance" testing

Design checklist to assess your design against EMC.

1. Design for EMC from the beginning; *know what performance you require; During the design/prototyping process, perform "precompliance" testing*
2. Partition the system into critical and non-critical sections
3. Select components and circuits with EMC in mind
4. PCB layout
5. Cabels
6. Grounding
7. Filters
8. Shielding
9. During the design/prototyping process, perform "precompliance" testing

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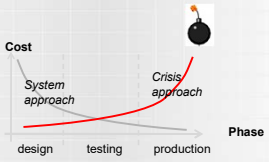
Design checklist to assess your design against EMC.
TIP 1:

- Design for EMC from the beginning; *know what performance you require; During the design/prototyping process, perform "precompliance" testing*

CE + CE = CE



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Design checklist to assess your design against EMC.
TIP 1:

2. • Partition the system into critical and non-critical sections:
   a)• determine which circuits will be noisy or susceptible and which will not
   b)• lay them out in separate areas as far as possible
   c)• select internal and external interface locations to allow optimum common mode current control

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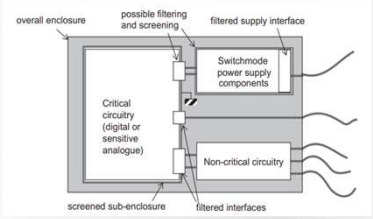

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Design checklist to assess your design against EMC.
TIP 3:

3. • Select components and circuits with EMC in mind:
   a) • use w and/or high-immunity logic; apply slew rate limiting to data transmission interfaces
   b) • use series R buffering on all high-speed clock and data lines
   c) • use good power decoupling techniques: small, low-inductance capacitors adjacent to the ICs they are decoupling
   d) • use series ferrite chips in the supplies to create power segments
   e) • reduce fan-out on clock circuits by liberal use of buffers
   f) • minimize analogue signal bandwidths
   g) • maximize dynamic range of analogue signal paths
   h) • check stability in wideband amplifiers
   i) • don't leave unused IC input pins floating: tie them to 0V or VCC
   j) • include resistive, ferrite or capacitive filtering at all sensitive analogue inputs
   k) • incorporate a watchdog circuit on every microprocessor
   l) • avoid edge triggered digital inputs if possible, protect them if unavoidable

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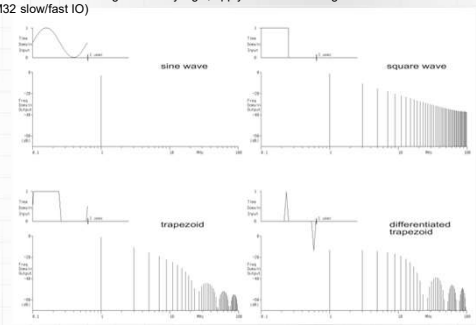
Design checklist to assess your design against EMC.
TIP 3: use slow and/or high-immunity logic; apply slew rate limiting to data transmission interfaces (e.g. STM32 slow/fast IO)



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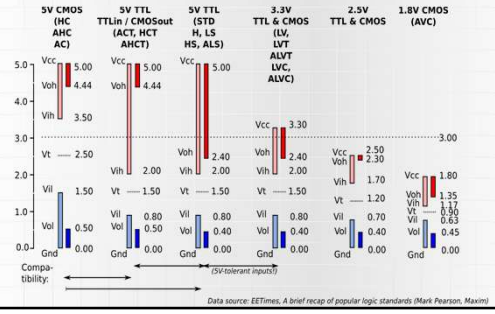
Design checklist to assess your design against EMC.
TIP 3:
use slow and/or high-immunity logic; apply slew rate limiting to data transmission interfaces



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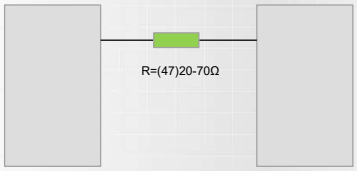
Design checklist to assess your design against EMC.
TIP 3:
use series R buffering on all high-speed clock and data lines



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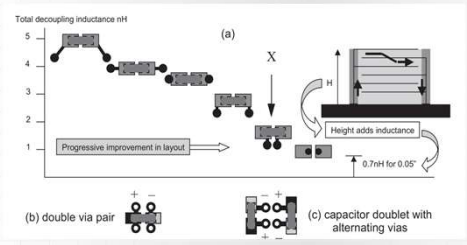
Design checklist to assess your design against EMC.
TIP 3: use good power decoupling techniques: small, low-inductance capacitors adjacent to the ICs they are decoupling



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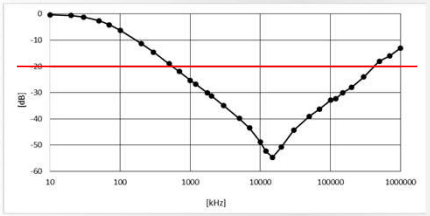
Design checklist to assess your design against EMC.
TIP 3: use good power decoupling techniques: small, low-inductance capacitors adjacent to the ICs they are decoupling



0.25Ω

Measured voltage gain for a SMD ceramic capacitor 10nF (Rgen=RVNA=50Ω)

22

$$Z = \frac{V_{CORE}*0.05}{I_{SUPP}*0.5} = 0.1* \frac{V_{CORE}}{I_{SUPP}}$$

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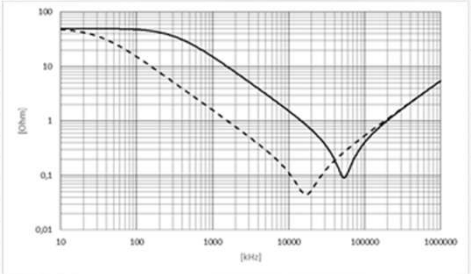
SMD Ceramic Capacitors



Impedance for a SMD ceramic capacitor 10nF and a SMD ceramic capacitor 100nF

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Design checklist to assess your design against EMC.
TIP 4:
• • PCB layout:
• refer to separate checklist in section about PCB design – next lectures

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Design checklist to assess your design against EMC.
TIP 5:
5. • Cables:
a)• segregate, and avoid parallel runs of, signal and power cables
b)• choose RF-screened cables if the wanted signal cannot be properly filtered
c)• avoid screened cable with the screen connected only at one end; if unavoidable, treat the cable as unscreened at RF
d)• use twisted pair both within and outside an enclosure, for balanced or high di/dt lines
e)• use properly designed looms, ribbon or flexi for internal wiring – avoid loose wires or bundles
f)• run cables away from apertures in the shielding, tied close to conductive grounded structures
g)• apply ferrite suppressors to damp resonances and control common mode currents
h)• ensure that cable screens are properly terminated to the connector backshell; avoid pigtails
i)• terminate lines carrying high frequency signals with the correct transmission line impedance

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- Class 4 Noisy: AC power and return, chassis ground, high-power RF and wideband signals; power inputs, outputs and DC links of adjustable speed motor drives, welding equipment, and similar electrically noisy equipment
- Class 3 Slightly Noisy: DC power, suppressed switched loads, filtered AC; externally supplied low-voltage AC or DC power which does not also supply other noisy equipment, contactor and solenoid coil circuits
- Class 2 Slightly Sensitive: low-power low frequency signals, low bit rate digital data; analogue instrumentation (e.g. 4–20 mA, 0–10V) and slow digital bus communications (e.g. RS232, RS422, RS485, Centronics); switched I/O such as limit switches, encoders, and the outputs of internal DC power supplies
- Class 1 Sensitive: low-level analogue signals such as thermocouples, thermistors, RTDs, strain gauges, load cells, microphones; also wideband digital and analogue communications such as Ethernet, video, RF receiver inputs; and all other signals with full-scale range less than 1V or 1mA, or with a source impedance > 1kΩ, or signal frequency > 1MHz

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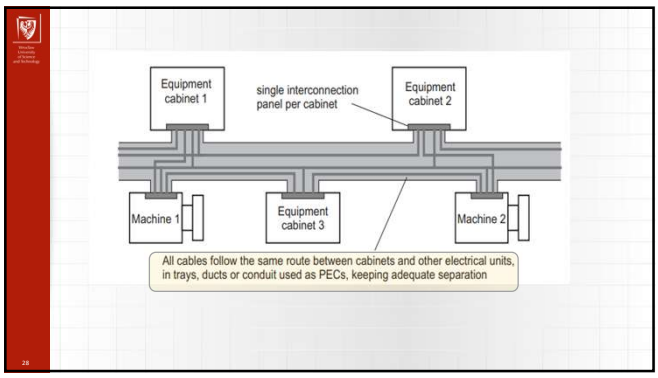
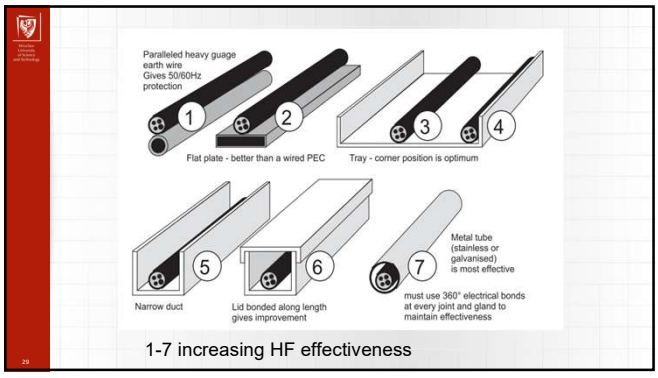
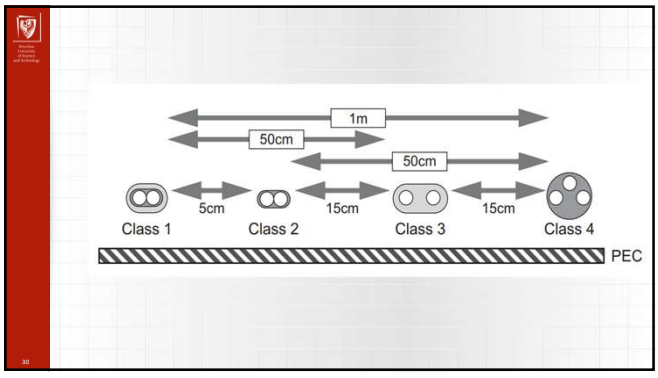




1-7 increasing HF effectiveness



EFFECT OF SHIELD ON MAGNETIC COUPLING
Magnetic Coupling - Open Wire to Shielded Conductor

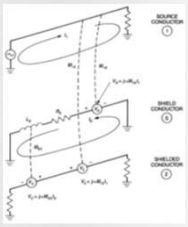
If the shield is **grounded at both ends**, the shield current flows and induces a voltage into conductor 2.

The total noise voltage induced into conductor 2 is

$$V_N = V_2 - V_{c'}$$

Note that ***these two voltages are of opposite polarity.***

$$V_N = j\omega M_{12} I_1 \left[\frac{R_S/L_S}{j\omega + R_S/L_S}\right]$$



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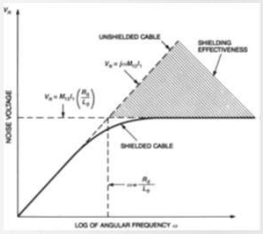
Magnetic Coupling - Open Wire to Shielded Conductor

The equation for V_N is plotted in the figure



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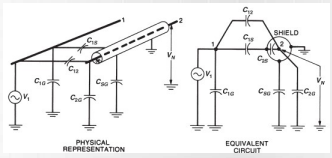
EFFECT OF SHIELD ON CAPACITIVE COUPLING

In many practical cases, the center conductor does extend beyond the shield, and the situation becomes that of the figure below



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EFFECT OF SHIELD ON CAPACITIVE COUPLING

For good electric field shielding, it is necessary
(1) to minimize the length of the center conductor that extends beyond the shield and
(2) to provide a good ground on the shield.

A single ground connection makes a good shield ground, provided the cable is not longer than one twentieth of a wavelength.
On longer cables, multiple grounds may be necessary.

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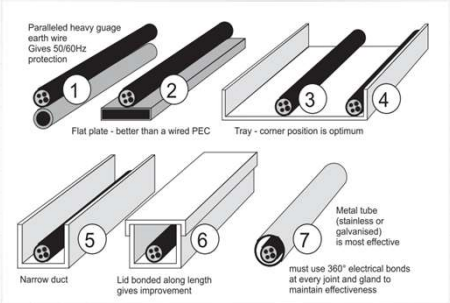

1-7 increasing HF effectiveness

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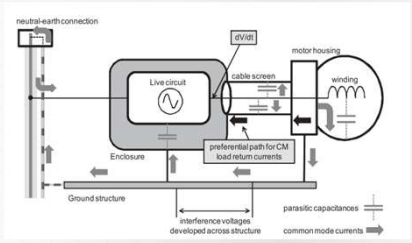
Inverter (VSD - variable speed drive)



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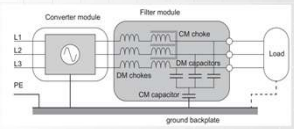
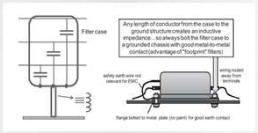
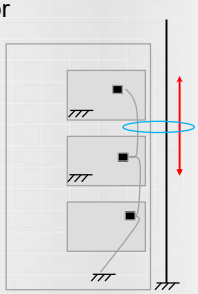




lightning conductor



Transfer impedance

Sample test questions:

1. What are the 3 interfering elements in EMC?
2. Sketch an example of the impedance of a real decoupling capacitor as opposed to an ideal one.
3. How can the transimpedance be described?

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